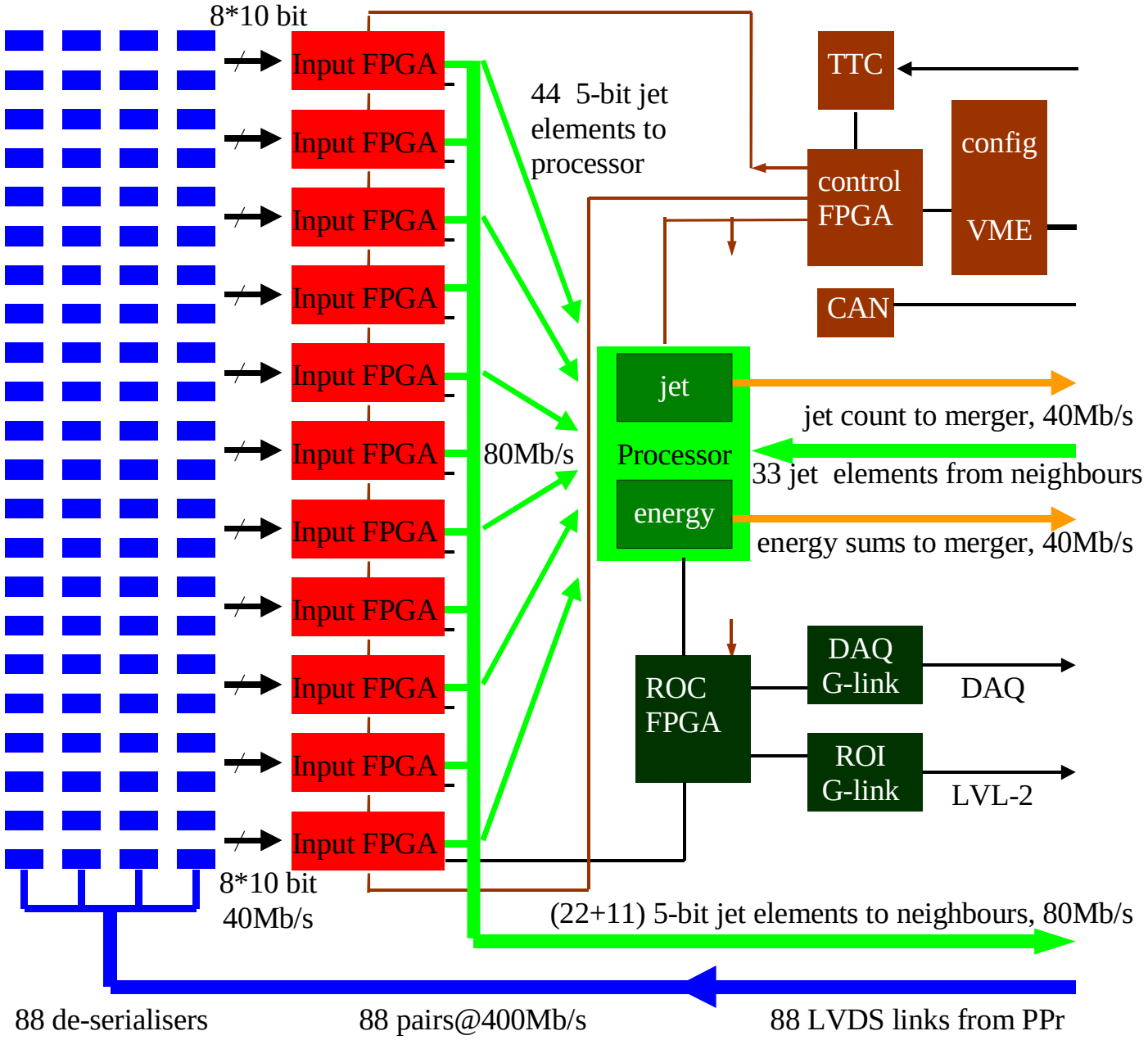
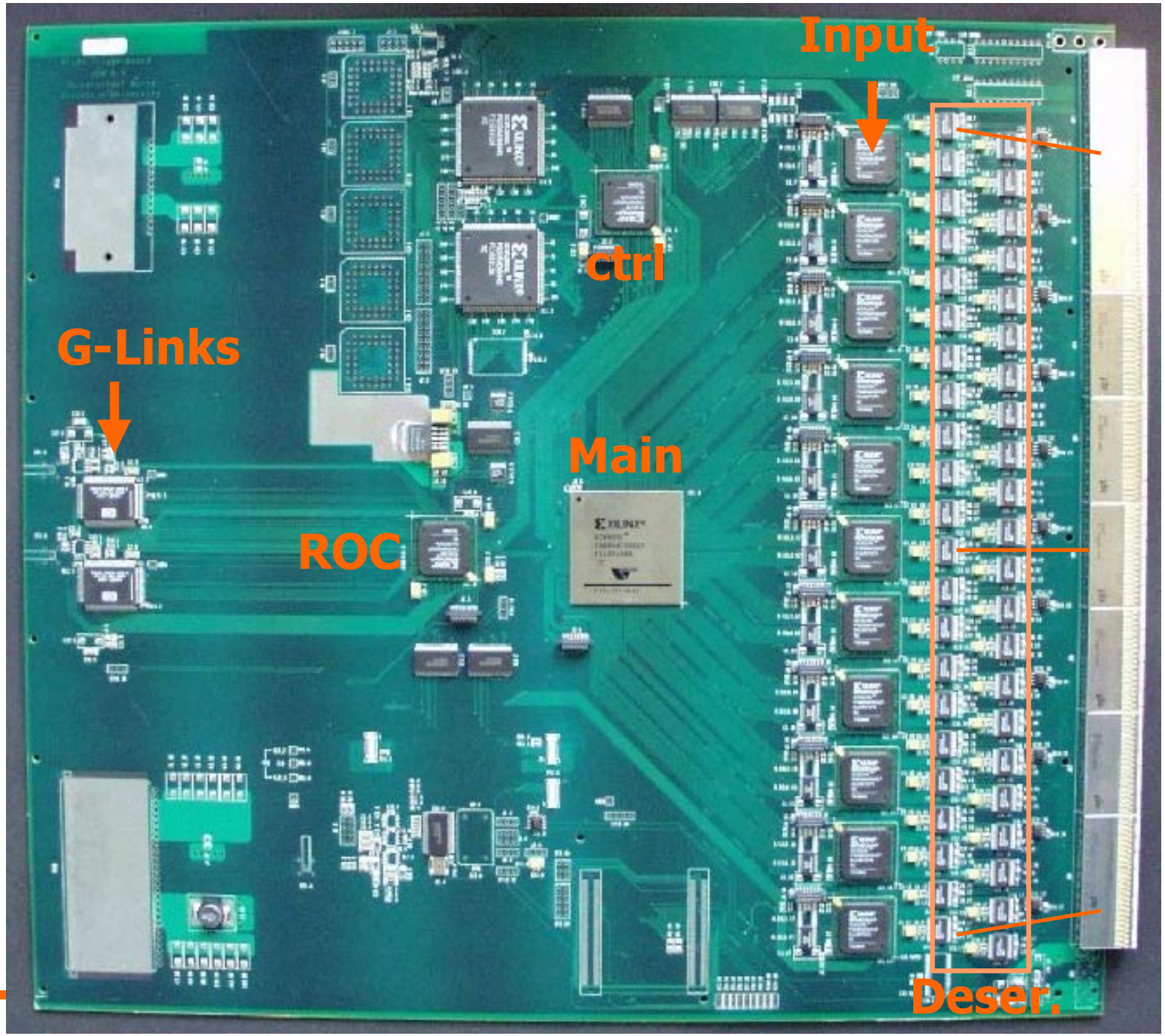
JEM0

- JEM0 Hardware : overview, history, and status
- JEM0 Firmware : algorithms, status
- JEM - The next iteration : many questions, few answers

JEM
-Block Diagram-



JEM0
-top view-



the JEM0 saga (1)

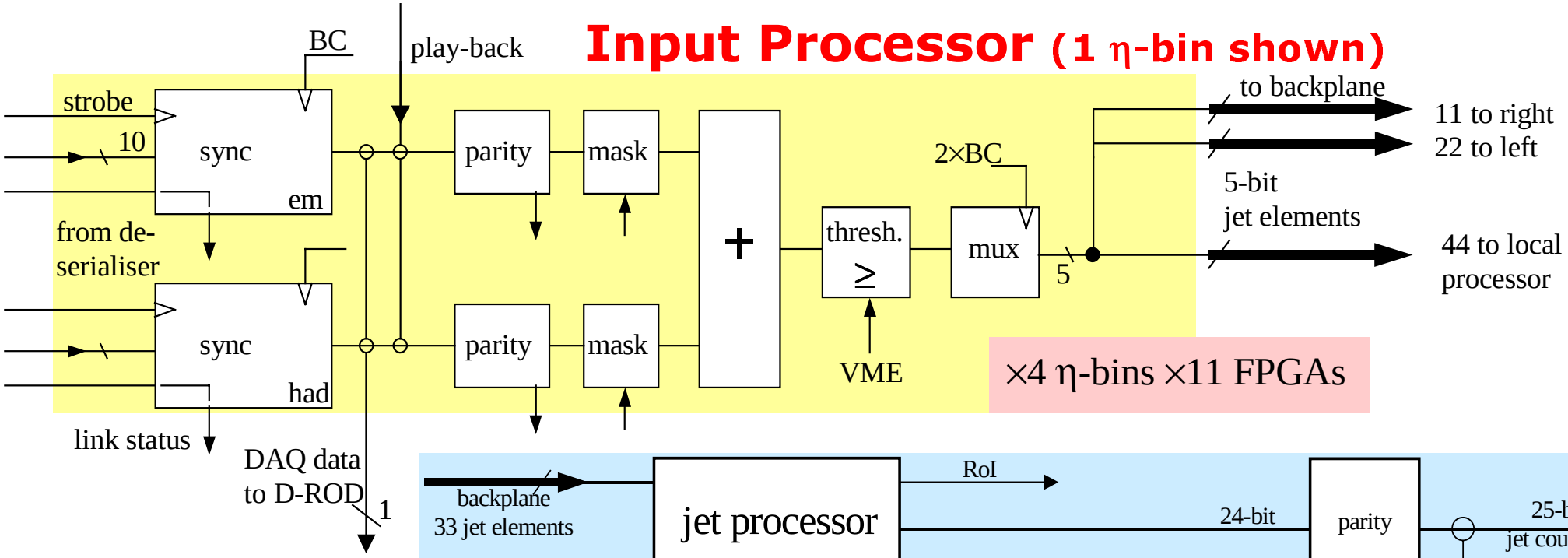
end 2000	JEM0 schematic capture and board layout
02.01.2001	board designs to PCB manufacturer (ANDUS)
31.01.2001	first PCB run failed
19.02.2001	second PCB run 'successful' : 1 PCB produced, 3 broken tracks
20.02.2001	some minor layout errors discovered, manually corrected.
06.03.2001	PCB and components sent out for assembly (MAIR)
25.04.2001	module received back with all Spartan-II chips rotated by 180° backplane connectors not very well aligned but probably ok.
27.04.2001	module sent for re-work (populate with spare chips). message from manufacturer: another chip failed, send a spare chip
29.05.2001	module received back with Virtex-E mounted incorrectly: Vcc short to GND. Possible reason: board too large, FR-4 boards tend to be mechanically instable at soldering temperature.
19.06.2001	module back in Mainz. Visual inspection shows no obvious problems. Start electrical tests
20.06.2001	JTAG chain doesn't work. Break chain to configure CPLDs.
26.06.2001	start work on configuration download path via VME

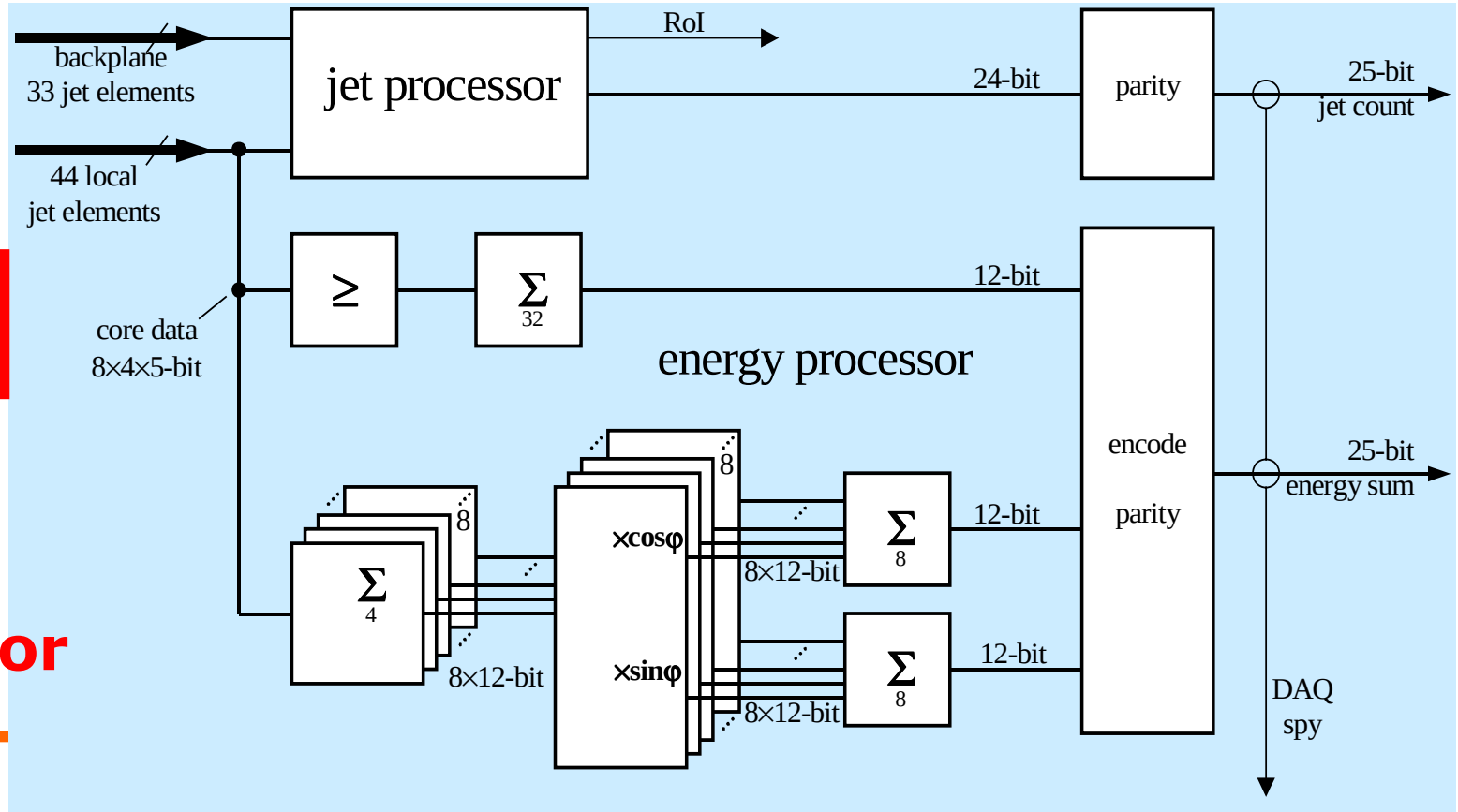
Observation: Input FPGAs apparently gone the way of all flesh

the JEM0 saga (2)

July	2001	discovered that the SpartanII are from an early production run not to final specs: they require a power-down signal for device startup which can not be applied on JEM0 board => it will definitely be impossible to configure the input FPGAs !
August	2001	JEM0 sent to Mair for re-work (-> SpartanII XC2S200)
October	2001	message from Mair: they feel unable to re-work the board and pass it on to Fraunhofer Institut in Hamburg. *No more hope. Earth to earth.....*
=>		Decision to have another PCB manufactured at Andus and have it assembled at Productware (they claim it is a simple job)
October	30th	Productware decide to pull out ! They feel unable to assemble that large a PCB (though we have kept discussing the board dimensions with them for weeks) !
		desperately seeking an assembler.....

Input Processor (1 η-bin shown)





Algorithms

Latency :
~4BC each

Main Processor

Firmware Status

No progress since July :

- VME CPLD carries a basic VME interface (almost finished)
- Input FPGA almost finished. Input synchronisation derived from the CP code at an early stage, might require update.
- Main processor: Top level and energy processor almost finished. Need to instantiate jet processor. FCAL handling will have to be modified due to revised allocation of FCAL channels.
- Control FPGA lacks TTC interface
- ROC code still missing, Andrea starting to work on that.

A lot of work to be done ! Lack of human resources.

considerations for Jem0.1

Board size **is** a problem !
We are using large and expensive high-density modules. Apparently the failure rate **is** high. We have to be prepared for re-work. Whenever we have a module in our hand we need to do connectivity tests as fast as possible.
To improve the turn-around time on our end we have purchased a JTAG/BS-tester (JTAG technologies (NL), parallel port adapter)

What else can we do to improve the situation ?
Should we reduce the size of seviceable/replaceable parts?
Since we rely on common modules, we cannot go for 6U modules, though JEMs could easily fit in 6U format. But:
We might be able to shrink module size by using daughter modules.
Even the mother board size could be reduced by CAMAC-style slide-mounted PCBs.
Virtex-2 will soon be available with 684 user-I/O in **1.28mm** pitch.
(XC2V6000-4BF957CES engineering samples currently available at **$ 4573.80**)

Will it make a difference?

-- *Whatever we do : it will drive up module cost ! --*

Serial link chips for JEM0.1

JEM0 carries 88 LVDS link chips, 44 each on solder side and component side of the 1.6mm thick PCB. This arrangement was chosen to minimise 480 Mb/s track length. However, problems experienced during vapour phase process might be related to insufficient stability of PCB

--> For next module iteration one might prefer a more rigid, thicker PCB
--> No LVDS link chips on solder side !

So as to keep LVDS tracks short we would have to go for higher density **compatible** deserialiser devices (Nat.Semi., Altera Mercury, Xilinx... ?)
Due to high component density JTAG/Boundary Scan highly desirable

1) DS92LV1260 6-channel compatible to DS92LV1021 no B/scan !

2) Mercury 8/18-chan. compat. to 92LV1021 (and HP G-link) firmware req'd !
3) Xilinx de-serialiser soft core too slow !
4) Xilinx Virtex-2 de-serialiser hard cores to be announced Q1 2002: too late !

--> *The only deserialiser likely to be available on our timescale is* DS92LV1260