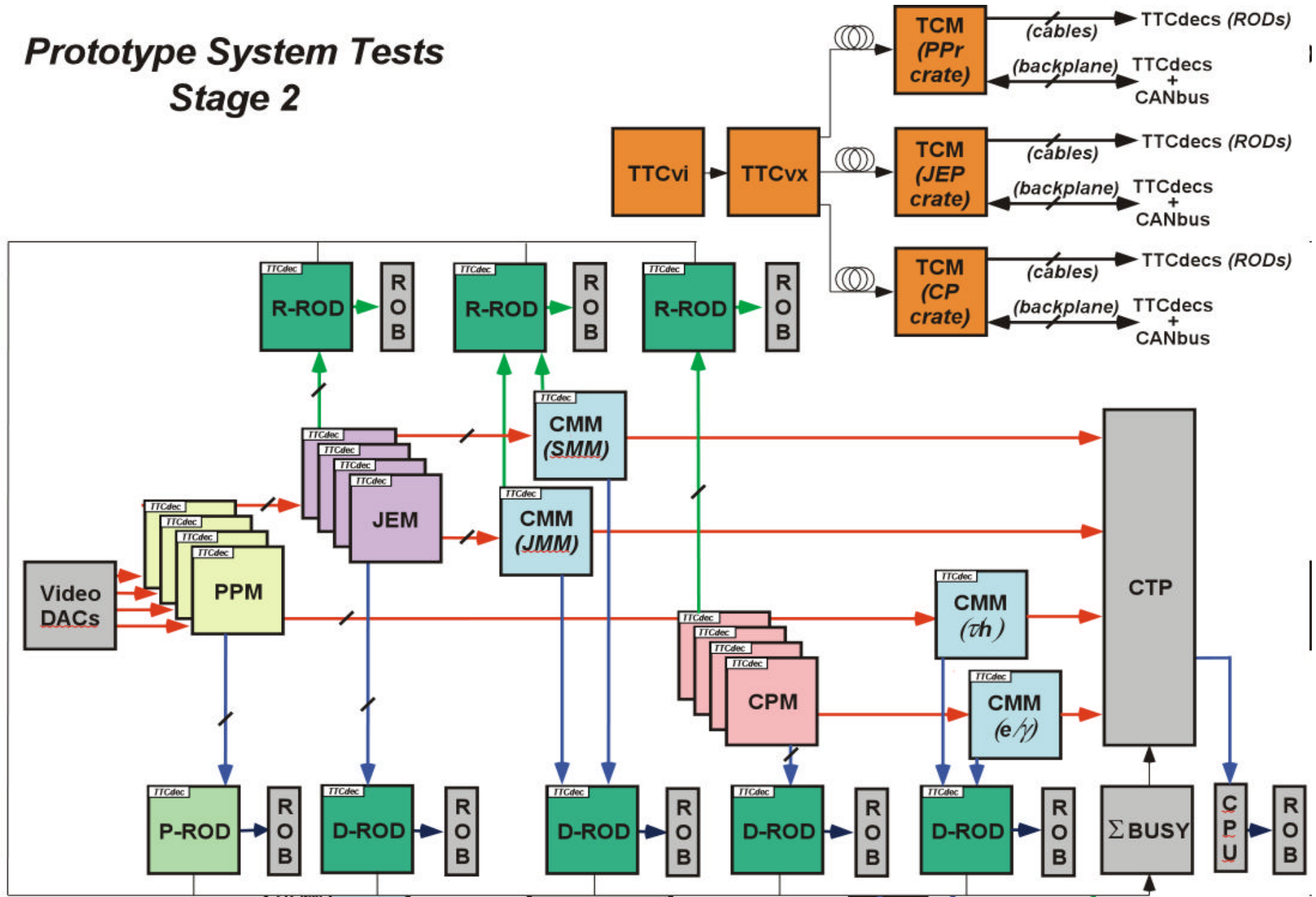10th October 2001

# Reading out the Slice.

C .N .P .Gee

Rutherford Appleton Laboratory

Prototype System Tests Stage 2

# Inventory

- **Pre-processor:timeslices from 4 Pre-processor modules via the Pipelinebus to PPRods, and then sent on to 1 S-link.**

- **4 CPMs. RoI and timeslice data is collected via separate prototype CPRODs onto 2 separate S-links;**

- **4 JEMs. RoI and slices sent to 2 S-links**

- **4 CMMs (2 CP + (2 Jet || 2 Esum || (1 Jet + 1 Esum))). RoI and slices sent to 2 S-links (library of 3 CPRODs).**

- **CTPD (see below). One S-Link**

- **DSS (see below)**

- **The TTC subsystem and TCMs. No readout, but do need control.**

- **Video DAC system - also needs no readout but does need control.**

# CTPD: Triggering & Readout

- **Triggering**
  - Start with TTC only, but use CTPD later as timing alters.
  - hard to control system if L1A from CTPD is generated by garbled hits from CMM when debugging the system.
  - therefore (at least initially) enable only 1 input bit to generate L1A, but still read out all 32 bits - of which say 30 from CMMs.

- **Readout**
  - timeslices go into a FIFO on the CTPD. There is enough room for ~ 2k 4-word timeslices.
  - Each event generates 1 to 5 timeslices (programmable).
  - A CPU with S-Link mezzanine must read, build, and send event fragments.

# CMM: Hit Outputs

- **CMMs together generate 98 data bits and 5 parity bits. Only 30 can be read by the CTPD.**

- **To read all the bits when the system is being driven from the PPr video memory requires special firmware in two DSS modules plus extra software and an extra S-link**

  - capture timeslices in DSS when L1A is received, then read both DSS modules by crate CPU and send as an S-link fragment.

- **Propose instead to rely on slice readout from the merger modules.**

  - With separate tests to ensure that this is equivalent.

  - This needs the extra firmware & software but not an extra S-link

# S-Link: Numbers and Data Rates (1)

| Source | Slinks | Data rate (Mb/s) |
|---|---|---|
| PPrs via PPROD | 1 | *100 (estimate)* |
| CPM Slice (4 G-Links) | 1 | 137.2 |
| CPM RoI (4 G-Links) | 1 | 12.4 |
| JEM Slice (4 G-Links) | 1 | *86.0 (estimate)* |
| JEM RoI (4 G-Links ) | 1 | 12.4 |
| CMM Slice (2 CP, 1 Jet, 1 Esum G-links) | 1(2) | *22 (estimate)* |
| CMM RoI (1 G-Link via CPROD) | 1 | 12.4 |
| CTPD via RIO CPU | 1 | 7.6 |
| **TOTAL** | **8 (9)** | **390.0** |

# S-Link: Numbers and Data Rates (2)

- **Assumptions:**
  - 100kHz L1A,
  - read one timeslice per L1A with or without zero suppression
  - 16 RoIs per event;
  - 4 words of data from CTPD copied directly to event fragment;
- **How to connect 8 S-Links to a PC**
  - S-Link to PCI interfaces or ROBIN boards.
  - use PCI expansion crate as only 3 PCI slots are available
  - link to the PC PCI by around 1m of cable.
  - Up to 13 slots can be added. Claimed speeds up to 132 Mbytes/sec.

# Requirements (1)

- **Read out one or a few modules at low and moderate rates for debugging. The system must stay alive when faults occur.**
- **Run at 100 kHz with DSS to check LVDS links (40 MHz).**
  - No need to analyse any events? Low rate errors?
- **Run at 100 kHz to soak test individual modules & small module chains.**
  - analysing a subset of events.
    - *How to choose the subset? Random? Highlighting some class of error?*
- **Software can check only a subset of events**
  - 20 kHz checking of RoI packets during the ROD integration test.
  - At 1kHz (guess), a 1 hour run samples 3.6 million events.

# Requirements (2)

- **Do we need more sensitivity than this?**
  - If so, we need to use DSS checking. It won't work with data from the video memories
  - But it is Hard to select events for computer checking or display based on DSS results.
- **There are two possible schemes for 100kHz running:**
  - using a ROD-crate DAQ system, sample events in the RODs.
  - use a ROS system. ROBIN modules are required to receive the events, and a subset are selected and analysed à la level-2..
- **Both schemes need software development. The ROS scheme (this talk) is similar to the one used in the Atlas test beam DAQ.**

# Access to ROBINs

- The ROS PC will not have the PCI bandwidth or CPU power to handle (read, build, monitor) events at 100 kHz.

- ROBIN modules receive fragments and buffer them, and expect software messages to delete or read out each event.

- RHUL is building ROBIN modules with ODIN-compatible input. We need one ROBIN for each S-Link (total 8).
  - *supporting software and firmware to run on the ROBIN modules;*
  - *supporting software in the ROS PC.*

- The slice test will use the ROBINs at a sustained 100kHz rate. This should be done in the UK in the first to check that it works.

# Selecting events

- **Need 8 DSSs to check all the PP, CP and J/E S-Link outputs.**
  - But it probably isn't necessary to check all outputs at the same time?
    - *The check can only be done with repetitive data - i.e. using the PPr replay memories, and part of the system at a time.*

- **Getting DSS mismatch messages to the ROS**
  - Run in Bursts of e.g. 100 events.
  - DSS crate CPU cehcks DSSs and sends "burst no 1234 OK" or "burst no 2135 bad" message to ROS (e.g. on another S-Link).
  - ROS reads message and discards all events in a good burst.

# How to Run

- Trigger using TTC

- Transmit Slice and RoI data over S-Links to ROBIN boards in a suitable PC running the ROS software.

- Use the TRG or Level-2 component of the ROS to pre-select a subset of events for event-building in the PC. Rejected events are deleted in the ROBINs.

- Build then distribute events to the event factory, for sampling by monitoring programs using the online monitoring skeleton.

- Histograms, if required, will be provided via T. Shah's ROOT software unless an alternative is available from Atlas.

# The End