CPM Prototype

Hardware Status

- Schematics
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  - Design Change
  - Spare pins
- PLDs
- Programming model
- Timescales

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Schematic Status:

47 A2 sheets!

Updated version now available on web at:
Thanks to James for his comments.

http://www.ep.ph.bham.ac.uk/user/staley/schematics/

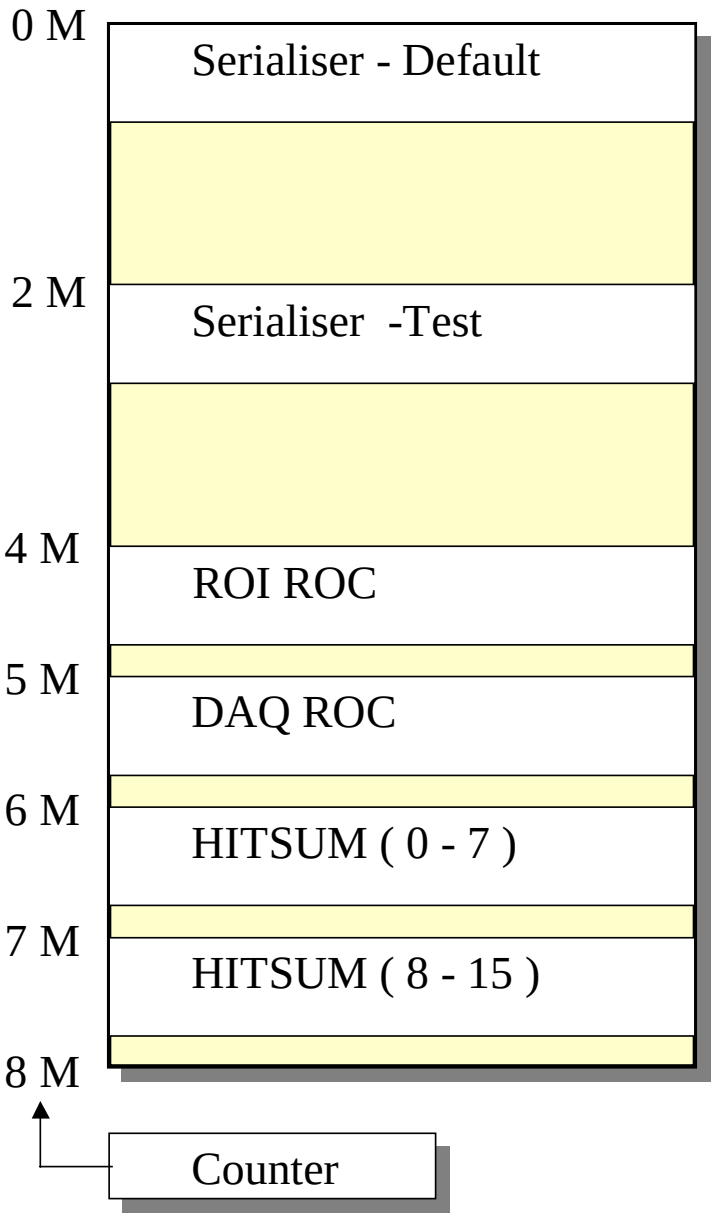
Index to CPM schematics

Thanks to James Edwards and Richard Matson for their help with publishing the schematics.
Updates to July 3rd Release: See below for links:
16/7/2001: Sheet 34, Configuration option from Serialiser FLASH added.
12/7/2001: Sheets 29 & 30, Controller clock was missing.
10/7/2001: Sheet 6, Buffers and bypass link added to TTCdec connector JTAG signals.
9/7/2001: Sheet 2, PCB Revision Number now hardwired to PCB (duh!)
8/7/2001: Sheets 34,36 & 37 JTAG cicuit gaffes corrected (well spotted JPE)
A tarredand zipped copies of all files below (except updates)

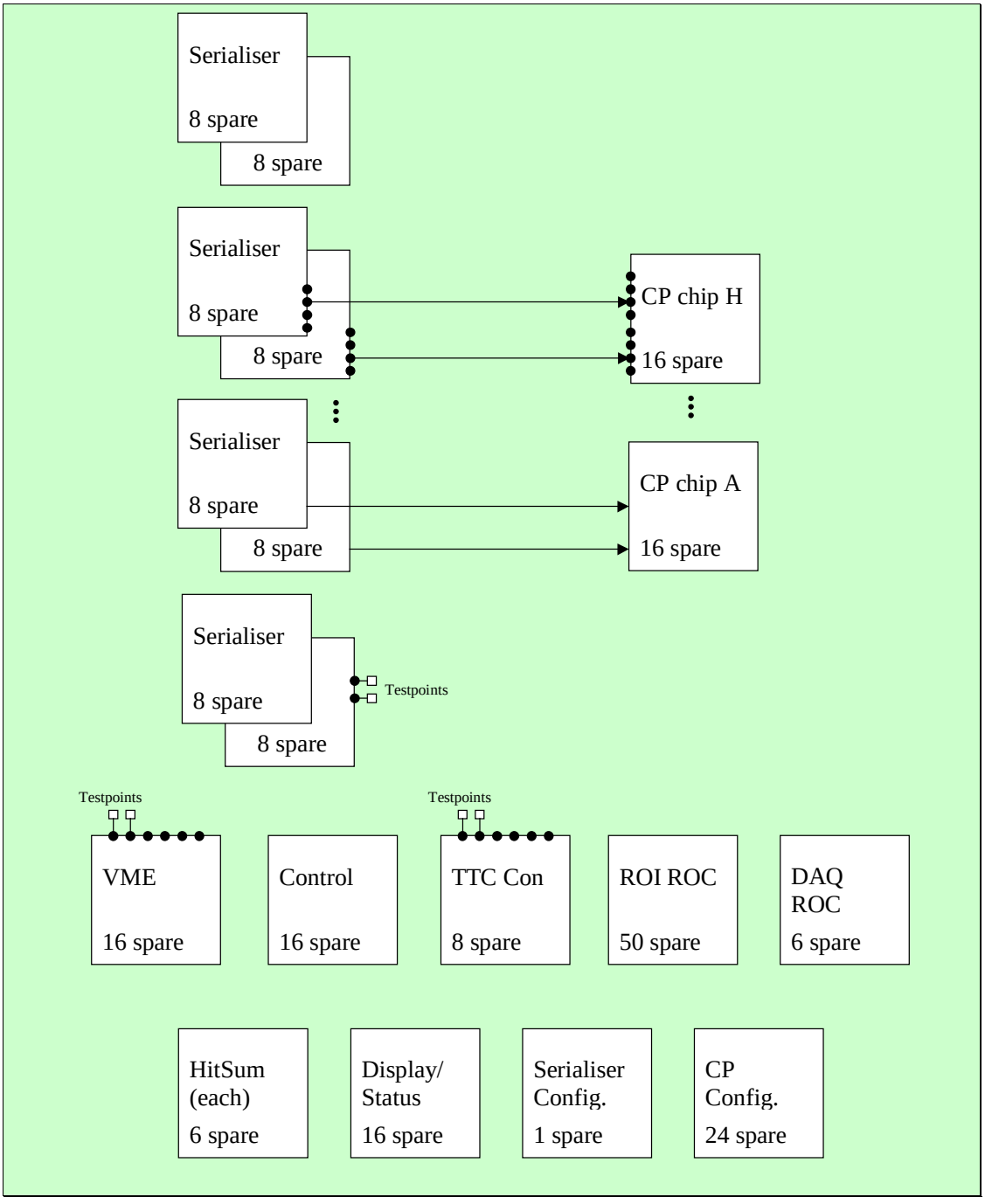
CPM Design Change

Serialiser Configuration store used a much under-utilised 8Mbyte Flash memory

- this now holds additional configuration for ROCs and HitSum FPGAs.



Spare pins:


Serialiser
8 spare
8 spare
Serialiser
8 spare
8 spare
CP chip H
16 spare
Serialiser
8 spare
8 spare
CP chip A
16 spare
Serialiser
8 spare
8 spare
Testpoints
Testpoints
Testpoints
VME
16 spare
Control
16 spare
TTC Con
8 spare
ROI ROC
50 spare
DAQ
ROC
6 spare
HitSum
(each)
6 spare
Display/
Status
16 spare
Serialiser
Config.
1 spare
CP
Config.
24 spare

FPGA / CPLD status

Function	Implementation	Status	
VME interface	Altera 3256A CPLD	VHDL prototype ✓ Pinout allocation ✓	☺
Control / Status CAN uC Status	Altera 3256A CPLD	VHDL prototype ✓ Pinout allocation ✓	☺
Ser . FLASH Configuration	Altera 3256A CPLD	VHDL prototype ✓ Pinout allocation ✓	☺
CP. FLASH Configuration	Altera 3256A CPLD	VHDL prototype ✓ Pinout allocation ✓	☺
LED Display Control	Altera 3256A CPLD	VHDL prototype ✓ Pinout allocation ✓	☺
TTCrx Interface With I2C Controller	Altera ACEX FPGA	VHDL prototype ✓ Pinout allocation ✓	☺
2 Readout Controllers	Xilinx XCV100EBG256 FPGA	VHDL prototype ✓ Pinout allocation ✓	☺
2 Hit Count	Xilinx XCV100EBG256 FPGA	VHDL prototype ✓ Pinout allocation ✓	☺

Programming Model

Current version available on web at:

http://www.ep.ph.bham.ac.uk/user/staley/cpm_memory_map.pdf

To be updated following comments received from Murrough.

Timescales

	Dates
Schematic Design finish	Mid July 2001
Detailed Programming Model	End June 2001
Layout finish	Mid Sept. 2001
Manuf. + Assembly 4 CPMs	Mid Oct. 2001
Module testing @ B'ham - Start	Nov. 2001
...	
Available for Slice Test	?????