

CPM Prototype

Hardware Status

- Schematics
 - Status
 - Design Change
 - Spare pins
- PLDs
- Programming model
- Timescales

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OF BIRMINGHAM**

Schematic Status:

47 A2 sheets!

Updated version now available on web at:
Thanks to James for his comments.

<http://www.ep.ph.bham.ac.uk/user/staley/schematics/>



Index to CPM schematics

Thanks to James Edwards and Richard Matson for their help with publishing the schematics.

Updates to July 3rd Release: See below for links:

16/7/2001: Sheet 34, Configuration option from Serialiser FLASH added.

12/7/2001: Sheets 29 & 30, Controller clock was missing.

10/7/2001: Sheet 6, Buffers and bypass link added to TTCdec connector JTAG signals.

9/7/2001: Sheet 2, PCB Revision Number now hardwired to PCB (duh!)

8/7/2001: Sheets 34,36 & 37 JTAG circuit gaffes corrected (well spotted JPE)

A [tarred](#) and [zipped](#) copies of all files below (except updates)

[Sheet1](#) - VME Address decoder and Address Buffers

[Sheet2](#) - VME Data buffers and Control/ Status Registers [Updated 9/7/01](#)

[Sheet3](#) & [4](#) - VME access to Serialisers

[Sheet5](#) - VME access to CP Chips

[Sheet6](#) - TTCrx Control [Updated 10/7/01](#)

[Sheet7](#) - TTCrx Clock Distribution

[Sheet8](#) - LVDS Rx + Serialisers VE and VH

[Sheet9](#) - LVDS Rx + Serialisers AE and AH

[Sheet10](#) - LVDS Rx + Serialisers BE and BH

[Sheet11](#) - LVDS Rx + Serialisers CE and CH

[Sheet12](#) - LVDS Rx + Serialisers DE and DH

[Sheet13](#) - LVDS Rx + Serialisers EE and EH

[Sheet14](#) - LVDS Rx + Serialisers FE and FH

[Sheet15](#) - LVDS Rx + Serialisers GE and GH

[Sheet16](#) - LVDS Rx + Serialisers HE and HH

[Sheet17](#) - LVDS Rx + Serialisers WE and WH

[Sheet18](#) - CP chips A & B , realtime data

[Sheet19](#) - CP chip C & D , realtime data

[Sheet20](#) - CP chip E & F , realtime data

[Sheet21](#) - CP chip G & H , realtime data

[Sheet22](#) - Hit Sum FPGAs

[Sheet23](#) - Hit Sum output drivers

[Sheet24](#) - ROI ROC + Glink

[Sheet25](#) - DAQ ROC + Glink

[Sheet26](#) & [27](#) - Serialiser Readout

[Sheet28](#) - CAN Controller

[Sheet29](#) - Serialiser Configuration Controller + Memory [Updated 12/7/01](#)

[Sheet30](#) - CP Chip Configuration Controller + Memory [Updated 12/7/01](#)

[Sheet31](#) & [32](#) - Serialiser Configuration bus

[Sheet33](#) - CP Chip configuration bus

[Sheet34](#) - ROC & Hit Sum Configuration + Power feed [Updated 16/7/01](#)

[Sheet35](#) - Indicators + Status

[Sheet36](#) - JTAG chains - Serialiser & CP Chip [Updated 8/7/01](#)

[Sheet37](#) - JTAG chains - TTC , remaining FPGAs [Updated 8/7/01](#)

[Sheet38](#) - Module Power Convertors

[Sheet39](#) , [40](#) , [41](#) & [42](#) - Serialiser Power feed

[Sheet43](#) & [44](#) - CP Chip Power feed

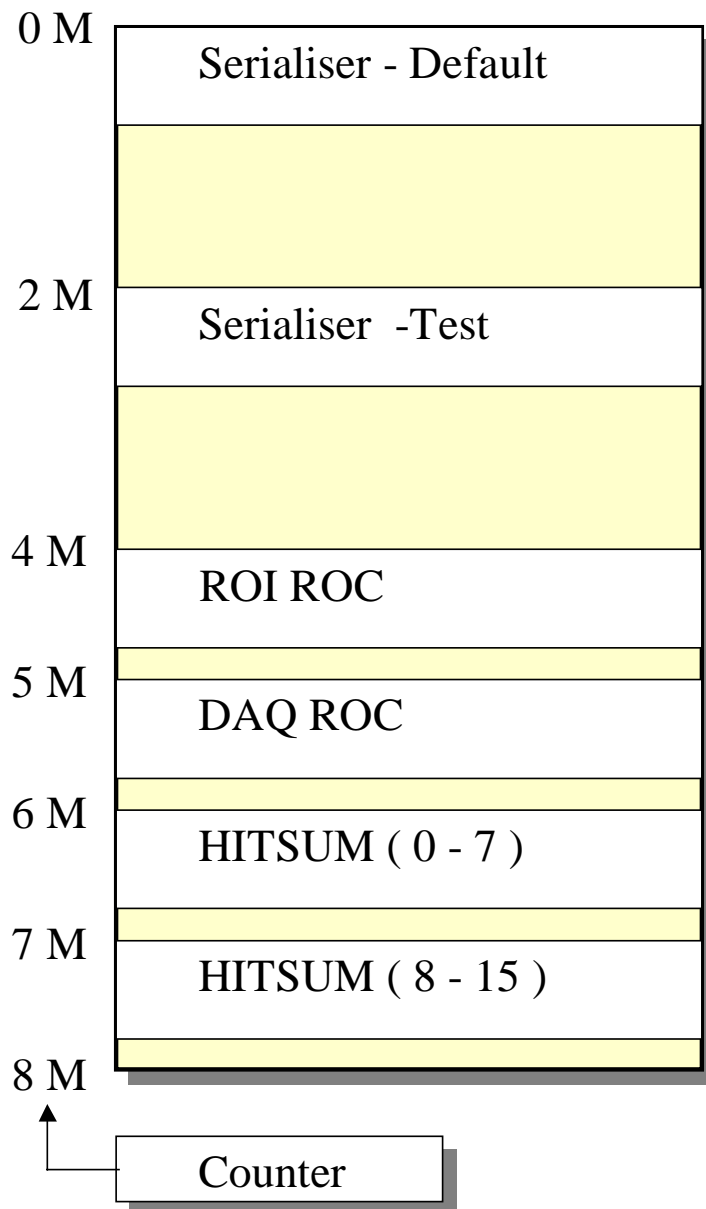
[Sheet45](#) - Backplane FIO signal name synonyms

[Sheet46](#) & [47](#) - Backplane connector

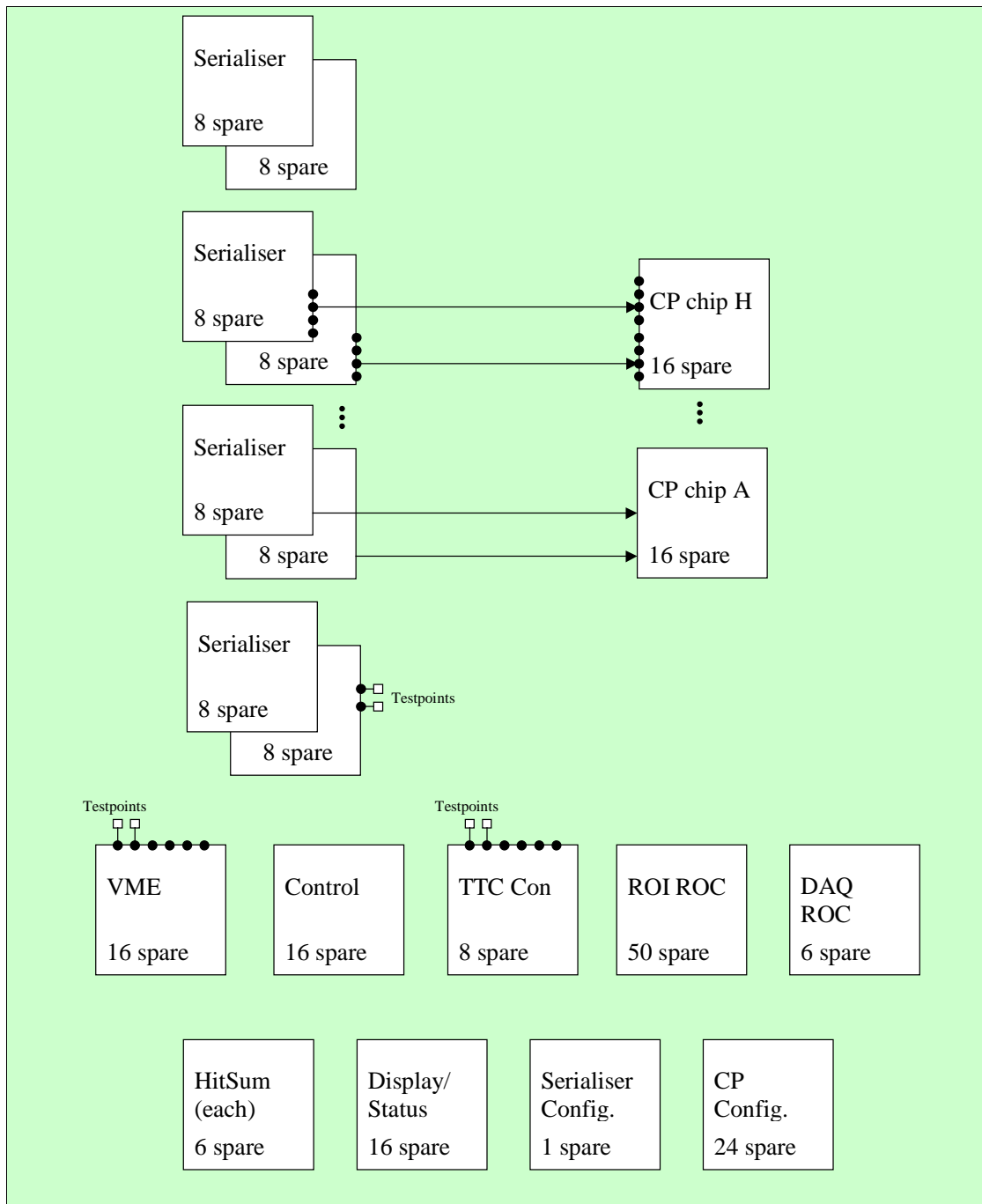
CPM Design Change

Serialiser Configuration store used a much under-utilised 8Mbyte Flash memory

- this now holds additional configuration for ROCs and HitSum FPGAs.



Spare pins:



FPGA / CPLD status

| Function | Implementation | Status | |
|---|-----------------------------|---|---|
| VME interface | Altera 3256A CPLD | VHDL prototype ✓ Pinout allocation ✓ | 😊 |
| Control / Status CAN uC Status | Altera 3256A CPLD | VHDL prototype ✓ Pinout allocation ✓ | 😊 |
| Ser . FLASH Configuration | Altera 3256A CPLD | VHDL prototype ✓ Pinout allocation ✓ | 😊 |
| CP. FLASH Configuration | Altera 3256A CPLD | VHDL prototype ✓ Pinout allocation ✓ | 😊 |
| LED Display Control | Altera 3256A CPLD | VHDL prototype ✓ Pinout allocation ✓ | 😊 |
| TTCrx Interface With I2C Controller | Altera ACEX FPGA | VHDL prototype ✓ Pinout allocation ✓ | 😊 |
| 2 Readout Controllers | Xilinx XCV100EBG256 FPGA | VHDL prototype ✓ Pinout allocation ✓ | 😊 |
| 2 Hit Count | Xilinx XCV100EBG256 FPGA | VHDL prototype ✓ Pinout allocation ✓ | 😊 |

Programming Model

Current version available on web at:

http://www.ep.ph.bham.ac.uk/user/staley/cpm_memory_map.pdf

To be updated following comments received from Murrough.

Timescales

| | <u>Dates</u> |
|--------------------------------|----------------|
| Schematic Design finish | Mid July 2001 |
| Detailed Programming Model | End June 2001 |
| Layout finish | Mid Sept. 2001 |
| Manuf. + Assembly 4 CPMs | Mid Oct. 2001 |
| Module testing @ B'ham - Start | Nov. 2001 |
| ... | |
| Available for Slice Test | ????? |