CPM Prototype

Hardware Status

- Schematics
- PLDs
- Timescales

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Schematic Status:

40 A2 sheets ≈ 90% completed:

Sheet no	Function	Status
1	VME Address decoder + address bus	
2	VME Data Bus + Module Control	
3 - 4	VME to Serialisers	
5	VME CP Chips	
6	TTC + clock distribution	
7	Serialiser Configuration Store	
8	CP Chip Configuration Store	
9 - 10	Serialiser Configuration access	
11	CP chip Configuration access	
12 - 21	LVDS Rxs + Serialisers V , A , B … H , W	
22 - 25	CP chips Realtime data path A B , C D, E F , G H	
26 - 27	Readout Serialisers	
28	ROC + G-Links Tx	
29	HIT logic (+ ROC)	
30	Module Power Convertors	
31 - 32	Serialiser Power connections	
33 - 34	CP Chip Power connections	
35	Indicators	
36	JTAG chains, Serialiser and CP chip	
37	JTAG chains, TTC + remaining FPGAs	
38	CAN Controller with signal conditioning	
39 - 40	Backplane connectors	

FPGA status

Function	Implementation	Status	
VME interface	Altera 3256A CPLD	VHDL prototype ✓ Pinout allocation ✓	☺
Control / Status CAN Interface	Altera 3256A CPLD	VHDL prototype ✓ Pinout allocation ✓	☺
Ser . FLASH Configuration	Altera 3256A CPLD	VHDL prototype ✓ Pinout allocation ✓	☺
CP. FLASH Configuration	Altera 3256A CPLD	VHDL prototype ✓ Pinout allocation ✓	☺
TTCrx Interface With I2C Controller	Altera ACEX FPGA	VHDL prototype ✓ Pinout allocation	☺
Readout Controller	Xilinx ??? FPGA	VHDL prototype underway Pinout allocation	☹
Hit Count	Xilinx ??? CPLD	VHDL prototype ✓ Pinout allocation	😐

Timescales

	Dates
Schematic Design finish	Mid May 2001
Detailed Programming Model	Mid May 2001
Layout finish	Mid July 2001
Manuf. + Assembly 4 CPMs	Mid Aug. 2001
Module testing @ B'ham - Start	Sept. 2001
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Available for Slice Test	?????