Design Reviews

1. Premiminary Design Review for the Pre-Processor Module *(PPM)* and Pre-Processor ROD *(PPROD)*

- **Draft 0.4 of the PPM specifications *(and first draft of the Line-Receiver daughter-board – AnIn – specifications)* from Paul Hanke et al**

N.B. These are "Module 0" *(pre-production)* designs

- **Draft 0.1 of the PPROD specifications from Bernd Stelzer et al**

N.B. This is a "Module –1" *(prototype)* design

- **Review Panel *(for both modules)*:**

  Bruce Barnett

  Eric Eisenhandler

  Steve Hillier

  Gilles Mahout

  Uli Schaeffer

  — supplied written comments in advance

- **Additional comments from Murrough Landon**

- **PDR held in Heidelberg on Thursday 8th March 2001**

- **Reviewers' comments addressed by Paul, Bernd *(et al)* in comprehensive written responses**
- **Usual number of minor amendments and clarifications to text and figures**
- **Amicable! – no unresolved disagreements about any significant points**
- ***(Hindsight)* – probably too much material to review thoroughly in a single day (*2.5 modules)***
- **Overall conclusions from the Review:**
  - ***The PPM is a well-specified design, feeding pre-processed real-time trigger data to the CP and JEP systems, and providing DAQ readout via Pipeline Bus***
  - ***Most of the functionality is in the Readout Merger FPGA (PPROD), and in the 16 MCMs (PPM) – separately reviewed***
  - ***The PPM and PPROD (and PipelineBus itself) must be considered as a single system***
  - ***The two interfaces (ReMFPGA and ROD Controller FPGA) are crucial to the readout performance, and possibly require a separate review together with the PipelineBus***

- ***More detailed conclusions (PPM - AnIn):***

1. **BC-MUX groups pairs of trigger towers in pairs in f – <u>not in h</u> (TDR section 6.3.1) – must be corrected by re-routing on the PPM MCM**

2. **Add table of power supply voltages (external and internally-derived) with estimated currents**

3. **Extend the JTAG chain to the ReM FPGA with an external port**

4. **Resolve (with Uli) the issue of End-Cap and F-CAL cable connections (groupings) for the PPM–>JEM links**

5. **Eliminate LFAN fan-out card for End-Cap/F-CAL by slightly extending Compact PCI connector and driving the extra signals from the main board**

6. **No fusing on individual module power supply pins – one board-level fuse per external power supply voltage is sufficient**

7. **Mapping of trigger towers to Pre-Processor crates should be clearly defined across the entire calorimeter trigger space**

8. **Investigate the stability of the AnIn LT1813 operational amplifier at a gain of 0.43 by reducing the gain further to establish the safety margin**

9. **Modified input resistor values in the FADC anti-aliasing filters must be tracked with similarly modified input capacitor values to ensure uniform -3dB filter roll-off points on all channels**

10. **Analogue BCID logic does not need a latching function to capture small amplitude signal glitches as this form of BCID is only utilised for saturated (large-amplitude) pulses**

11. **The board ID should be at address 0 (system convention), and a system-wide solution to ID allocation must be sought**

12. **Increase initial number of PPMs to be constructed *(for the Slice Tests)* to four**

- ***More detailed conclusions (PPROD):***

1. **A more detailed description of the PipelineBus should be added, as it forms the core of the readout system**

2. **The readout data should be defined as 1 BCID slice and 5 raw data slices maximum**

3. **The modified Huffman encoding algorithm will provide a factor of ~2.5 data compression – this statement should be clearly emphasised (and justification given)**

4. **PipelineBus data transfer error measurements have been extensively studied – the excellent bit-error rates (<10^{-14}?) should be clearly highlighted**

5. **A front-panel LED should be added to indicate when ROD BUSY is asserted**

6. **The board ID should be at address 0 (system convention), and a system-wide solution to ID allocation must be sought**

7. **"Dynamic" registers (Status, Control, …) will be implemented in the VME CPLD**

8. **+ . . .**

2. Final Design Review for the Pre-Processor Multi-Chip Module *(PPrMCM)*

- **Draft 0.1 of the specifications written by Ullrich Pfeiffer**
- **Review Panel:**

  Christian Bohm

  Eric Eisenhandler

  Viraj Perera

  Philippe Farthouat (CERN)

  (representing ATLAS Technical Coordination)

  — supplied written comments in advance

- **Additional comments from Uli Schaeffer**
- **FDR held via video and audio conference on Thursday 12th April 2001**
- **The usual minor amendments and clarifications to both text and figures discussed and agreed**

- **Review Summary:**

  - ***The PPrMCM is a well-engineered design, with a long history of successful development stages***

  - ***The recommendations from the Preliminary Design Review have been adopted in almost all cases***

  - ***Details of the test programme are still evolving – appropriate interaction between the Heidelberg group and the assembly company is crucial***

  - ***Failure rates will remain unknown until the first pre-production devices are sampled***

  - ***Ullrich Pfeiffer's departure is a major concern – close monitoring of the assembly procedures for the initial devices will be essential***

  - ***Philippe Farthouat's participation as ATLAS TC representative was very important – his comments will be valuable to simplify the PRR***

- ***Some of the more detailed conclusions:***

1. **The LVDS low-speed (<40 MHz) serialiser dies selected for the pre-production devices may need to be upgraded to the high-speed (>40 MHz) variants for production *(LHC clock – 40.08 MHz)***

2. **The maximum tolerable jitter for the LVDS serialisers is quoted as 150 psec, believed to be tighter than that guaranteed by the TTCrx – must be checked, and PLL added to PPM if necessary**

3. **Although NS recommend multiple decoupling for the LVDS serialisers (1/10/100 nF), real-estate limits the MCM to a single 10 nF per serialiser – extra capacitors must be added at board-level**

4. **Procedure for replacing defective FADCs by mounting new dies above old dies is acceptable (~industry-standard) – needs care (grounding, …)**

5. **MCM MTBF calculations are highly sensitive to individual die failure rates – nominal figures give 8% MCM failures/year ® 72% PPM failures/year!**

6. **Burn-in of individual dies is not planned – careful study of the first 64 pre-production MCMs will indicate whether reliability would improve sufficiently to justify the extra complication**

7. **The choice of 12-bit FADCs is justified by the improvement in ENOB figure – this should be further explained**

8. **Test Plan for initial devices is still evolving with assembly company – several issues to be defined, e.g. envelopes of parameter tolerances, liability for failures and associated re-working**

9. **Care must be taken to use appropriate die-attach material, e.g. do FADC dies need Ag-loaded adhesive? These details must be precisely specified to assembly company**

10. **As the MCMs will not have fully-hermetic seals, the silicone gel must prevent moisture ingress – MCM/PPM storage must be in dry N_2 cabinet/bags**

11. **The recommended current limits should be checked for the proposed 25 μm Al bond wires**