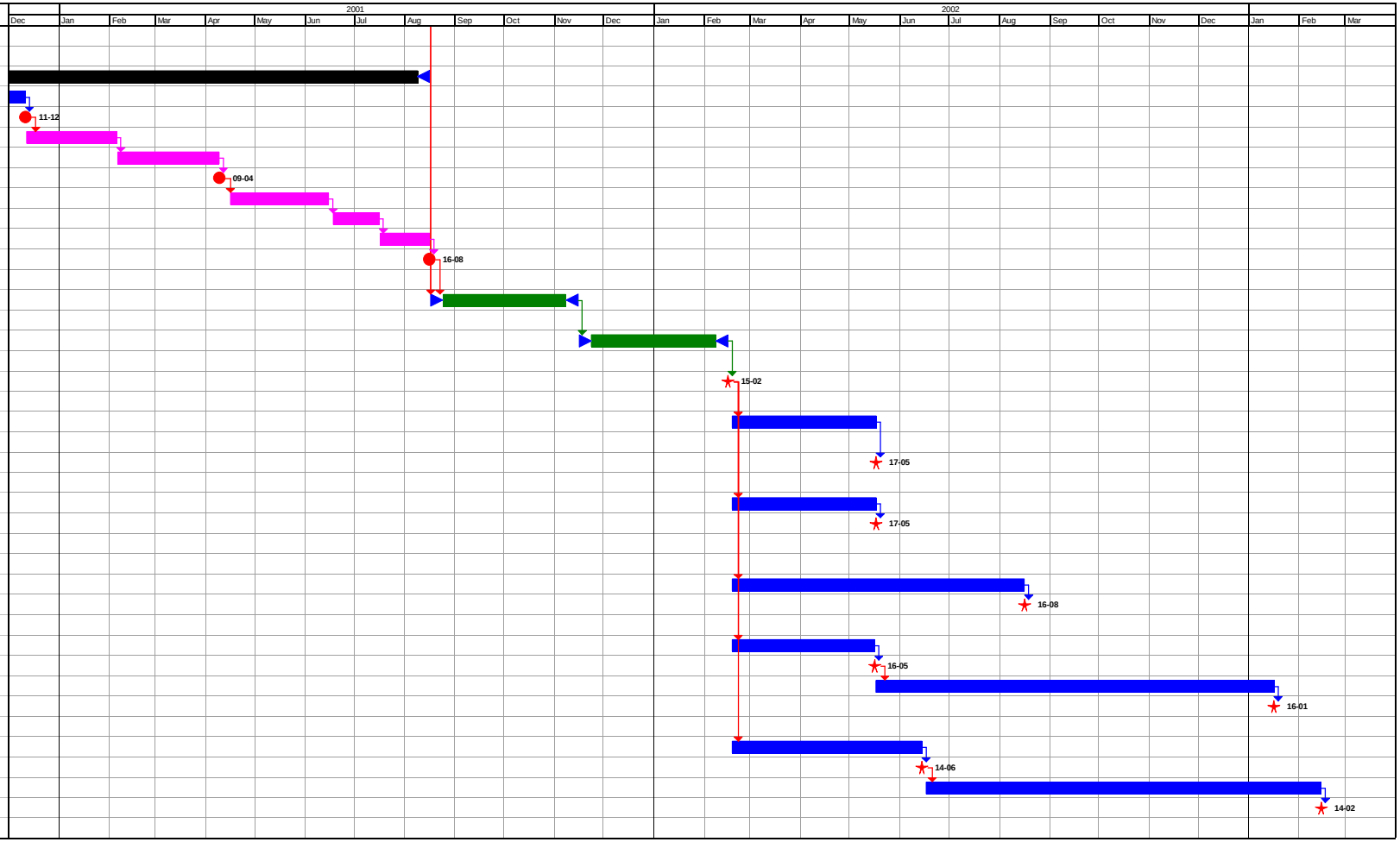
ID	Task Name
1	
2	***CP System Design Programme***
3	
4	**P-ROD Prototype**
5	Layout
6	Manufacture
7	Engineering tests
8	System tests (P-ROD/D)
9	Prepare RoI FPGA code (P-ROD/R)
10	System tests (P-ROD/R)
11	***P-RODs available for sub-system tests***
12	
13	**TCM Prototype (including Adapter Link Card)**
14	Design
15	Schematic review
16	Layout
17	Manufacture
18	Standalone tests
19	***TCMs available for all sub-system tests***
20	
21	**P-Backplane**
22	Specifications
23	PDR
24	Layout
25	Manufacture
26	Standalone tests
27	***P-Backplanes available for sub-system tests***
28	
29	**GTM (Generic Test Module)**
30	Specify
31	***PDR***
32	Design
33	Layout
34	Manufacture
35	Standalone tests
36	***GTM available for CP/Serialiser FPGA tests***
37	
38	**CP-FPGA**
39	Specify
40	***PDR***
41	Design firmware
42	Test with Serialiser FPGAs (using GTM)
43	***CP/Serialiser FPGAs available for CPMs***
44	
45	**CPM Prototype**
46	Specify
47	***PDR***
48	Schematic design
49	***Schematic review***
50	Layout
51	PCB manufacture
52	Assembly
53	JTAG tests (RAL)
54	Standalone tests (Birmingham)
55	***CPMs available for CP sub-system tests***

ID	Task Name
56	
57	
58	**Common Merger Module (CMM)**
59	Specify
60	***PDR***
61	Update specifications
62	Schematic design
63	***Schematic review***
64	Layout
65	Manufacture
66	Standalone tests
67	***CMMs available for sub-system tests***
68	
69	**CP sub-system tests - 3 months**
70	
71	**Phase 1 "Slice" tests (Heidelberg) - 3 months**
72	
73	***Phase 1 "Slice" tests complete (Milestone)***
74	
75	CPM design iteration
76	
77	***CPM Final Design Review/PRR (Milestone)***
78	
79	Backplane design iteration
80	***P-Backplane FDR/PRR (Milestone)***
81	
82	
83	CMM design iteration
84	***CMM Final Design Review/PRR (Milestone)***
85	
86	TCM specifications (Module-0)
87	***TCM PDR (Milestone)***
88	TCM pre-production design phase
89	***TCM FDR/PRR (Milestone)***
90	
91	P-ROD specifications (Module-0)
92	***P-ROD PDR (Milestone)***
93	P-ROD pre-production design phase
94	***P-ROD FDR/PRR (Milestone)***
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