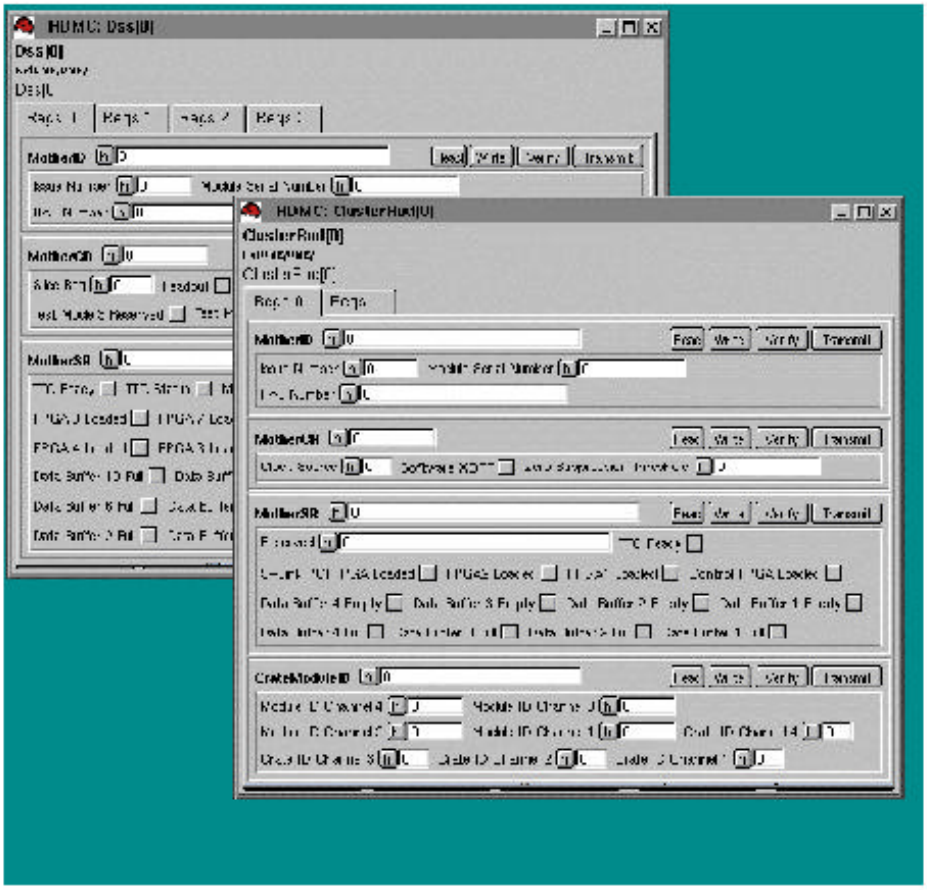
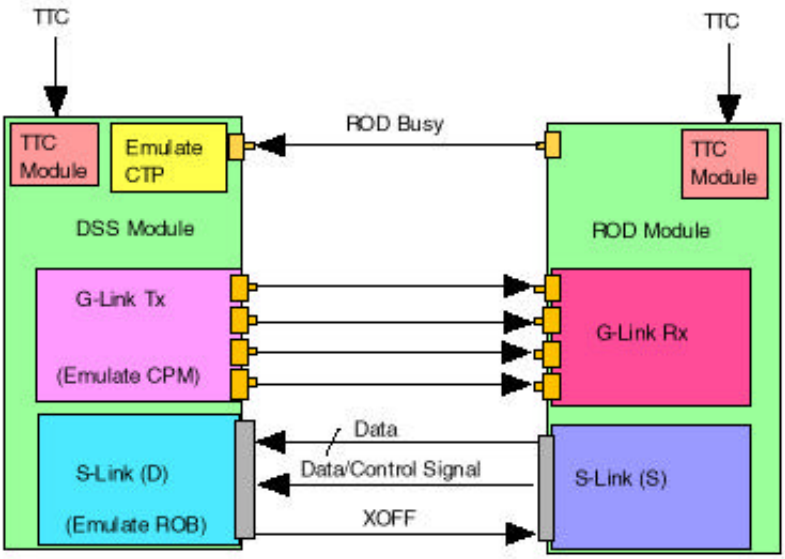
News from the Rutherford Trenches

1) Diagnostic and DAQ software under development:

- In the last month, not much s/w progress to report.
- Some work invested in the module-to-buffer manager part of this code.
- Current status of readout-level DAQ code is HDMC enhanced with DAQ-classes:



2) First Level ROD Tests:



a) Tests with onboard clocks confirmed basic operation under ROD Test Plan: (http://www.te.rl.ac.uk/esdg/atlas-flt/test_plans/rod/test_plan1-2.pdf)

- Generated Data transfer into fifos on ROD.
- Transmission of this data back into ROD.

b) Next stage incorporated:

- TTC distributed clock.
- L1A to trigger data transfer.

Status:

- The use of the ROD Pulse Register to reset ROD FIFOS, while using theTTC Clock results in G-link reset and a subsequent flooding of FIFOS.

- This is under investigation, but occurs regardless of whether Clock40, Clock40Des1, Clock40Des2 (with a variety of “fine delays”).

- Tests Stalled.

Side Benefits:

- Experience in TTCrx setup and TTCvi use, as required for control in subsequent tests.

Observation:

- Use of Module-view GUI in combination with DAQ classes is more comfortable than is the use of raw unstructured register collections (DAQ classes).

- Some script development for HDMC based tests has indicated the usefulness of the scripting features. It is flexible but not fast, as the script parsing is not particularly intelligent in helping to locate syntactic errors.

3) Priorities for s/w given upcoming tests …

- Integration and further evaluation (so that Bill can consider extensions) of Bill's test-vector Generator (TVG) needs to be done soon. What additional features are needed?

- Integration of buffer-manager, DAQ-classes, TVG should proceed with more urgency: March tests at CERN, verification of ROD functionality).

4) New Hardware:

- Norman will order a new PIII class PC (Athlons are nicer). RH7.0 to be installed.

- Murrough has specified new VME systems for order:

  Concurrent Technologies VP PSE/P34-17, which is a single slot 850MHz Pentium III board with 256 Mb RAM and a three row P2 connector with SCSI transition module included.

- Birmingham to order 1, RAL 2.

5) Outstanding issues:

- There have been some requests for s/w resource sharing with groups outside of L1 Cal. Trigger (eg: Stephano Veneziano @ Rome). What is the best way to integrate such requests with our program, commitments, the ROD-DAQ plans, etc?

- Worrysome News from the East. No. Terrifying news from the East. Critical S/W Effort in Heidelberg is evaporating. What does this mean regarding the DAQ/Diagnostic dependence on HDMC? How will HDMC be supported?