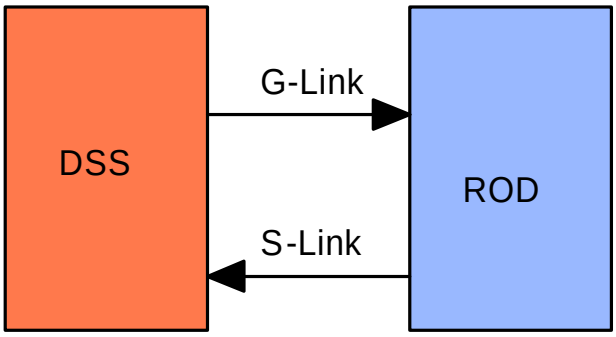
Prototype ROD Status as at 23/01/2001

- Two modules assembled and tested in R25 Lab



- Test Plan on the web (http://www.te.rl.ac.uk/esdg/atlas-flt/)
- One test set-up installed in R1 Lab with the TTC system
  - Problems with TTCrx decoder connectors on the board (connectors swapped over)
    - Small PC card made to correct the problem
  - Problems with the Pulse Register
    - Should generate pulse only if bit is set

- DSS firmware modified to select between:
  - CP Slice data and RoI data
  - Internal clock and TTC clock
  - Internal L1A and TTC generated L1A

- Firmware for the prototype ROD

Function	Design
CP Slice	Done
CP RoI	Done
JEM Slice	
JEM RoI	
CMM _CP Slice	1
CMM_Jet Slice	2
CMM Et Slice	3
CMM Et RoI	4

    - Combine designs 1 & 2 and designs 3 & 4 to use one ROD per combination.
    - Four more designs to do.
        - If the format is given (as in CP RoIs) then RAL can do the designs (preferred)

- Two more modules will be assembled after few more tests in R1 lab
- Two (four) PCBs and components need to be ordered for slice test requirements.
    - Total of six (eight) prototype ROD modules.
- S-Links ordered
    - 6 x ODIN Double LDC 5V (680-1110-950-5LDC2)
    - 6 x ODIN Double LSC 5V (680-1110-950-5LSC2)
    - Delivery March/April 2001