



3rd September 2002

Heidelberg, Mainz & Stockholm Status



C .N .P .Gee
Rutherford Appleton Laboratory



Heidelberg - Paul



- **Karsten has completed his thesis. MCM tests show digital output consistent with the input analogue pulse, but the parity seems wrong when the digital data are all zero. He will join the HD group after a pause to recover, and do systematic MCM tests to check digital output with analogue input from the video memory.**
- **Ralf is developing VME tests of ASIC using Labview. So far the ASIC is in default power-up mode, (no register access yet).**
- **Paul is writing PPr C++ code within the simulation framework, needed to interpret digital output from the MCM.**
- **Some equipment has been moved to the technical building. The main move will be on 16/17 September.**



Mainz - Uli



- **A new DSS daughter board with the 6-channel LVDS receiver chip has been designed and is ready for manufacture. LVDS links will be tested using the new chip before using it in the JEM in place of the existing 4-channel device.**
- **Original LVDS test was done by Richard with the old diagnostics. Two pairs of Tx/Rx cards coming to RAL for testing with HDMC and current DSS (with many firmware changes). Then send a tested Tx/Rx pair to Mainz. Uli already has two LVDS Tx cards. Paul will send four 15m LVDS cables to Uli.**
- **LVDS card pinout doesn't match the existing AMP cable – to document.**



Mainz (2)



- **When LVDS test is complete, JEM studies will be resumed. The 80MHz paths on the JEM have been timed-in, and the readout firmware rewritten to match the latest slice formats.**
- **Andrea has driven signals down the G-Link, which locks at the receiving end, but the data has not yet been checked.**
- **Three of the real-time tracks are broken on JEM-0.**
- **The loop-back test board has been manufactured and awaits populating.**



Stockholm - Sam



- **Sten is now resident in Stockholm.**
- **Attila has improved on the Jet algorithm firmware speed from. 65 or 74 MHz to 110 MHz by changing comparators to be fully parallel and adding extra flip-flops (+12.5 ns).**
- **The design will be back-annotated, then tried with test vectors.**
- **A JEM + crate etc could then be used in Stockholm. RAL to check on the status of the box sent recently.**
- **Daniel and Asa have decided to work within the common simulation framework.**



End



The End