# Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 6th May 2004


***Birmingham:*** **Gilles Mahout, Richard Staley, Pete Watkins**

***Heidelberg:*** **Ralf Achenbach, Florian Föhlisch, Christoph Geweniger, Paul Hanke, Eike-Erik Kluge, Katja Krüger, Kambiz Mahboubi, Karlheinz Meier, Pavel Meshkov, Frederik Rühr, Klaus Schmitt, Hans-Christian Schultz-Coulon**

***Mainz:*** **Uli Schäfer, Andrey Belkin**

***QMUL:*** **Eric Eisenhandler, Murrough Landon, Jürgen Thomas**

***RAL:*** **Bruce Barnett, Ian Brawn, Norman Gee, Tony Gillman, Weiming Qian**

***Stockholm:*** **Christian Bohm, Sam Silverstein**


## *1. Birmingham*

- Testing of the two new CPM1.5 modules has been continuing.
- Problems have been seen with apparently corrupted data on some pins of some of the CP chips, only with the new PCBs (CPM1.5). The data are received by the chips correctly as the input signals appear normal when probed on their vias, and also are observed to be OK when temporarily routed to spare pins for 'scope observation.
- This problem got worse (more pins affected) when Gilles modified the CP firmware to use the second backplane clock, so it suggests some marginal timing problem associated with the firmware.
- Gilles is trying to use ChipScope to diagnose what is happening, but at present there are no available global clock distribution resources in the CP chip.
- Gilles' "2-backplane clock" CP chip firmware appears to work so far, but no attempt at optimisation has been made.
- Tamsin visited Birmingham on Wednesday this week to test her firmware patches for the Serialiser, which fix the zero-data parity error in the old PPr ASIC. Two different techniques have been coded, and both operated correctly when tested on a single Serialiser channel. The same piece of code will now be added to the CP chip to operate in the real-time data path.
- Richard is ready to start the schematics design of the LSM (LVDS Source Module) next week.

## *2. Heidelberg*

- Bench tests on PPM#1, instrumented with four MCMs (16 channels), have been continuing successfully. VME access has been working correctly for some time. The I2C interface to the ASIC also works, and the next stage will be to write data to the ASIC.
- A lot of work is going into coding the firmware for the PPM ReM FPGA.
- Two assembly companies have been assessed on visits, and quotations are awaited for assembly of the next three PPMs. One of the companies has already produced good-quality work on a similar board.
- A list of minor PCB revisions is being updated as they are found, and these will be incorporated into the layout for the final production boards.
- The latest batch of 50 MCM substrates (more than expected), using FR4 material, has been delivered from Würth. Visually the substrates appear to have a very good surface finish, and they have now been sent away to be pull-tested for bond strength.

- The first 60 brass lids for the MCMs are being made in the KIP workshops using a numerically-controlled machine. Finally, all ~5,000 lids will be made in-house in the same way.
- Layout of the LVDS fan-out daughter-card, which uses the large I/O capacity of two FPGAs, is currently at the final routing stage, but the very high track density has caused some problems. When finished, four daughter-cards (for the four PPMs) will be manufactured by Würth.
- Tests of the new ASIC mounted on one of the old MCM substrates have continued, and all functions tested so far are working well. Recent tests have covered the FIR filter and BCID logic. The histogramming function still needs to be tested.
- The proposed date of June for the ASIC/MCM PRR remains feasible, but a final decision awaits completion of all necessary tests on both the ASIC and the MCM.
- The first re-designed AnIn (Analogue Input) daughter-card is assembled and ready to be tested, and another five PCBs are available for assembly once the design is confirmed. For the Slice/Beam Tests, AnIns of the original design will be used, accepting the 5% crosstalk between certain channel pairs.
- There was some discussion about the location of the TileCal Patch-Panels, following a request for information from Bob Stanek. An offline phone discussion will be held between Paul, Murrough and Tony to agree the rack locations, and Murrough will put the final layout on the web, as well as ensuring that Philippe Farthouat's database is updated.
- Florian spent last week at QMUL working with Murrough to prepare the PPM database.
- Frederik described the plans for their participation with PPM#1 interfaced to the LAr and TileCal receivers in the June Test-Beam run at CERN. The schedule has been delayed by a week due to a PS Booster water leak, but the visit will still take place starting on June 7$^{th}$. The first week will be spent setting-up and using the "scrubbing" beam period, with the data-taking during the second week (14$^{th}$ – 21$^{st}$ June) when the 25nsec beam will be present.
- It will probably now not be possible to carry out the LVDS interfacing tests with the CPM until after the June Test-Beam run, i.e. after June 21$^{st}$, but this is very close to the Collaboration meeting in Stockholm which starts on June 30$^{th}$, which is immediately followed by the first phase of the DAQ integration at RAL during the week beginning July 5$^{th}$. A proposal for when and where (Heidelberg, Mainz or RAL?) to carry out these important interfacing tests will be prepared as soon as possible..
- The plan is to make the additional three PPMs available for tests after the 21$^{st}$ June, but the availability of people as well as hardware must be considered.

### *3. Mainz*

- As yet there is no understanding of the cause of the burn-out of the JEM0 module.
- The replacement G-link daughter-cards will be ready in about one week from now.
- One of the JEM1 Input daughter-cards has a broken connection to one of the FPGA balls, which was an assembly problem caused by using PCBs which had been stored for too long.
- A strange fault has been seen on three of the recent batch of Input daughter-cards, where all pins on an FPGA are in their tri-state (high-z) state after configuration. It appears to be position-dependent, i.e. a function of the location on the PCB. Unfortunately, the effect is intermittent, and currently not reproducible.
- Testing the firmware functionality requires some work to be done on the on-line software, which will take a few days.
- A further three JEM1 modules are ready for assembly, once JEM1#1 is fully-tested.

### *4. RAL*

- Placement of all components for the 9U ROD is now complete, and routing has started. The layout should be completed by the end of May, assuming no serious problems.
- 9U ROD firmware development: Ian has partitioned the Input FPGA so that the data reception from G-links, and the data preparation for the FIFO buffers (internal to the FPGA) in the S-link format, are separated from the common logic such as the FIFO buffers themselves, the control logic, VME registers, etc. James is back at RAL now and he will handle the firmware for the Switch FPGA that will interface to the S-Link cards and the Input FPGAs. So Ian will be the link between the front-end data reception, handled by Weiming, Dave, etc., and the back-end Switch. Ian will also code the firmware for the Monitor FPGA, and Adam will handle the VME firmware.
- It is planned to incorporate the ROD firmware designs into the Synchronicity environment soon
- The CMM is now able to control its TTC timing via VME.

### *5. Stockholm*

- Sam has modified the CPM hit-merging firmware for the CMM, supplied by Ian, to operate with jets. He is now writing the necessary code to incorporate forward jets. He has made good progress with the crate-level summing code, but the system-level summing is more difficult.
- The re-designed prototype Backplane hardware, including the new power distribution bus-bar system, is complete. Tony will arrange for the Wiener 9U crate to be shipped from RAL to Stockholm next week for mechanical trials. The power cables to each crate slot have a cross-section of 2.5 mm2, and the maximum length of 5 cm needs to be checked for acceptable IR drop.
- The proposed dates for the backplane FDR and PRR are August and September 2004, which at present appear to be achievable.

**Next Phone Conference – Thursday 20$^{th}$ May 2004 at 10:00 (UK), 11:00 (Germany, Sweden)**

***Tony Gillman***