Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 11th November 2004

Birmingham: **Richard Booth, Stephen Hillier, Gilles Mahout, Richard Staley**

Heidelberg: **Ralf Achenbach, Florian Föhlisch, Kambiz Mahboubi, Karlheinz Meier, Pavel Meshkov, Klaus Schmitt, Hans-Christian Schultz-Coulon**

Mainz: **Stefan Rieke, Uli Schäfer**

RAL: **Bruce Barnett, Tony Gillman, Viraj Perera**

Stockholm: **Sam Silverstein**

1. Birmingham

- Gilles reported that the modified CPM firmware, allowing the operation of the G-links with two independent clocks, works correctly.
- The problem of VME access to one of the CP-chip registers, seen at CERN, no longer occurs, so is believed to have been caused by the damaged VME-- connector in the Processor crate TCM slot.
- There is a problem with one of the original CPMs (CPM#1), where the flash memory reads back corrupted configuration data.
- Richard reported that the order to manufacture two new CPMs (version 1.9) has been placed, and the expected delivery date to RAL is December 20th 2004.
- Quotes have been requested for the manufacture of two LVDS Source Modules (LSMs). An estimate should be made of the final total number, for use with the CPMs and JEMs.

2. Heidelberg

- Hans-Christian reported that a total of 48 wafers of PPr ASICs had been ordered, in two batches of 24 wafers. Unfortunately, the first batch had been damaged at the foundry, and four wafers from the second batch had also been lost, so only 20 wafers had been delivered to KIP. The projected yield requires a further 21 wafers, which will be delivered to KIP on December 21st 2004.
- The four MCMs – 2 with silicone gel filling, and two with glob-top encapsulation – have been subjected to 20 temperature cycles over the range 25 – 80 degrees Celsius, after which all four devices are still working normally. A further 80 cycles will be carried out with the upper temperature limit extended to 100 degrees Celsius.
- Kambiz noted that the PPM problems continue to be studied, and a full report on their status will be presented at the Birmingham meeting. He said that the problem of I2C access to the PHOS4 chips on the PPM MCMs had been solved, but that the TTCdec card still had an apparent addressing problem for non-zero I2C addresses. Both Uli and Richard commented that they had not seen this problem with non-zero addresses on the JEMs and CPMs. (After the meeting, Viraj suggested that this effect could possibly be caused by an insufficiently wide Reset pulse.)

3. Mainz

- Uli reported that the problem seen at RAL of being unable to configure two of the JEMs was caused by the System ACE CPLD apparently corrupting the crystal clock. Swapping to using the clock from the TTCdec fixed the problem, but the cause of the problem is not fully understood. Monitoring of the clock does show rather poor signal quality on these two particular modules. Uli also noted that JEM configuration problems had also been observed when using clocks with very fast edge speeds.
- One of the two TTCdec cards sent to RAL from KIP will be shipped to Mainz.
- More TTCdec will be manufactured immediately, as at least 15 will be needed within the next month (4 PPMs + 4 CPMs + 4 JEMs + 3 RODs – plus some spares). Therefore a further ten cards will be

ordered, making a total of 20 available. The necessary TTCrx chips have already been requested and will be at RAL next Monday (15th November).

- Uli asked if there had been any problems observed with the use of System ACE at RAL. Viraj replied that the system would not operate at 20 MHz, but reducing the clock frequency to 10 MHz was successful. Uli noted that the situation was similar at Mainz, but that the addition of bus driver devices allowed operation at 20 MHz.

4. RAL

- Viraj reported that the VMM and TCM schematics are now available on the web at:

  http://www.te.rl.ac.uk/esdg/atlas-flt/

- The order to manufacture two CPM1.9 modules had been placed, with delivery expected on December 20th 2004.
- The manufacture of the LSMs was awaiting a quote from one of the "one-stop shop" companies.
- The 9U ROD had experienced problems with establishing G-link lock, caused by the G-link receiver getting into an inactive state at start-up during the FPGA configuration phase, which could not be cured even by a reset. This had been traced to the DIV0 pins on the G-link receivers being driven from the Input FPGAs and having undefined logic levels during this phase. The temporary solution has been to hard-wire these pins to logic zero, but they may need register control when switching between 16-bit and 20-bit operation. Ian and Adam are now starting to send G-link data into the ROD from a DSS module. Using Chipscope, Ian observes that all control signals to receive the data and write to the FIFOs are present, so the next stage is to use VME to verify the integrity of the data received from the DSS.
- The Framework contract for pcb manufacture and assembly is now in place at RAL, with the EU tender exercise successfully concluded. Three suppliers have been selected.
- Bruce noted that he had sent out a summary of the integration tests at RAL last week, which included a CMM test with a heavily-loaded backplane. The next imminent stage of CMM testing will use two cable-linked Processor crates, as requested by the recent CMM FDR.

5. Stockholm

- Sam reported that he had released the draft of the Processor Backplane FDR documentation, and that the FDR itself would be on December 6th 2004 at RAL. The recent RAL test results (see above) will be added to this draft document.
- He is having discussions with three companies regarding manufacture of the production Processor Backplanes, and would be ready to go out for tender immediately following the FDR.
- Sam also noted that Weiming had successfully replaced a broken Processor Backplane connector pin using the AMP repair tool.
- It was noted that the JEM FIO tests should be carried out soon – probably at RAL – with every pair of Processor crate slots exercised. Hopefully, this can take place in the week beginning 29th November 2004.
- He also reported that he has started to look into the cable management problems in the TileCal Patch-Panel crates, and we will discuss this issue further at the Birmingham meeting. Steve noted that Bill Cleland has started to develop some ideas for cable management in the LAr Receiver crates, which we should follow up.

Next Phone Conference – Thursday 9th December 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman