Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 13th February 2004

Birmingham:	**Steve Hillier, Gilles Mahout, Richard Staley**
Heidelberg:	**Karlheinz Meier et al**
Mainz:	**Cano Ay, Stefan Rieke*, Uli Schaefer***
QMUL:	**Eric Eisenhandler*, Murrough Landon****
RAL:	**Bruce Barnett, Ian Brawn, Norman Gee, Tony Gillman, Weiming Qian**
Stockholm:	**Sten Hellman, Attila Hidvegi*, Sam Silverstein***
	***at RAL** ***at DESY**

1. Birmingham

- During the RAL tests, three CPMs have been used to successfully read out five data slices per event to a ROD, in long runs.
- RoI data have also been transferred, but only in short (~15 minute) runs. In this configuration, the G-links frequently lose lock.
- The TTCdec cards apparently produce a high level of clock jitter, which is a serious problem for G-link stability. There are various questions about the TTCdec version, the TTCrx chip package, whether the jitter is seen also on the JEM0 or CMM, … .This problem must be investigated urgently if long data-taking runs are to be possible.

2. Heidelberg

- A useful phone meeting was held between Heidelberg, RAL and Pittsburgh to discuss the worrying behaviour of the LAr Rx module to saturated pulses. It was agreed to: a) increase the dynamic range, b) change the low-pass filter time constant from 15 nsec to 5 nsec. When these changes have been made, the saturated pulse measurements will be redone. Bill will visit Heidelberg ~4/5 March.
- The MCM substrates from Wurth, although optically showing poor bond pad surface finish, exhibit good bond pull strength. However, the pre-substrate test structures from the Swiss company demonstrate the reverse – optically good, but with poor bond strength.
- The reason for the poor yield (~30%?) of “good” substrates from Wurth is still unknown.
- Two non-working MCMs from the original batch have been returned from Hasec after rework (PPr ASIC replacement). They are ready to be re-tested.
- Fabrication of the new PPr ASIC wafers is scheduled for completion in Week 11 (mid-March?).
- The first PPM PCBs are scheduled to be back at Heidelberg by 18th February, where they will be assembled with components.
- One further PPM daughter-card is still needed – the LVDS fan-out module, which is being designed now by Klaus, and should be ready for manufacture in two weeks. Testing of the PPM can initially go ahead without this daughter-card.
- The G-link Rear Transition Module will also be needed in about two weeks time. This can be discussed further at the forthcoming Collaboration Meeting in Heidelberg.
- Automated test software for the new PPr ASIC and MCM has been prepared by Pavel, and is almost ready.
- There will be a meeting with Wiener to discuss the ordering of the VME64x(P) crates in about 10 days, after Paul returns.

3. Mainz

- The JEM1 PCB layout is complete, and assembly is scheduled for Week 9 (early March?).
- The JEM1 Input FPGA is currently being tested.
- About 20% of the new 6-channel LVDS links lock correctly, and the data are error-free, although only with limited statistics at present. To make high-statistics BER measurements (<10**-12), the parity error bit can be scaled with a counter.
- For the energy-sum processor, sections of code need to be merged, and the CPLD code for the VME interface has to be rewritten, but it should all be ready in time for JEM1. I2C-handling code will be obtained from Ian.

4. QMUL

- Eric reported that the 9U VME64x crates had finally been ordered from Wiener via CERN, and delivery dates of June and November 2004 defined. The use of VME64xP backplanes for the ROD crates had been avoided by some rearrangement of the +5V power distribution.

5. RAL

- The three TileCal Patch-Panel (TCPP) modules have been assembled at Birmingham, and will be tested for connectivity and crosstalk soon.

Tony summarised the status reports received from Viraj, who was unable to be at the meeting.

- 9U ROD: The DC-DC supplies had to be changed due to ripple noise. The Drawing Office has started the layout of the sub-section that deals with the optical receiver, Lemo sockets, LEDs and associated components and started to look at the front panel. It requires some “tweaking” to fit everything into the front panel area as shown in the specification. The next sub-section, which deals with the 4 G-links and the Input FPGA, will be passed to the Drawing Office ~now, and it is hoped that the rest of the checking will be complete at the latest by the middle of next week. Ordering the components for three RODs awaits quotes.

- CPM1.5: This is on schedule so far, with PCBs expected in the first week of March. Mechanical samples from Xilinx are needed by the assembly company for the temperature profiling of the module, and will cost approximately £1200. This will be sufficient for all the samples we require for the CPM, CMM and the RODs. However, negotiations continue to see if Xilinx will offset this cost when the production devices are bought.

- DSS: One of the two DSS modules that failed JTAG testing when they long ago came back from assembly has been made to work by Adam.

- Backplane connectors, etc (Sam’s e-mail): We already have ~1000 guide pins. Some of the backplane connectors we use on the CPM and CMM are from Harting. It appears that AMP, Erni and Harting manufacture similar parts. Viraj suggests that the requirements for all our modules are put together and a request made to various manufactures for price, minimum order quantity and delivery. A single order should then be placed (to meet MOQ) as we have done for other common items.

6. Stockholm

- Functionality of the CMM central jet algorithm is about to be checked.
- During the tests at RAL, JEM RoI data have been transferred to the ROD, but some firmware modifications are needed to ensure correct event synchronisation.
- Additional Jet FPGA firmware will be needed for JEM1.
- For the processor backplane, ERNI can apparently provide a second source of high-current power/ground pins and mechanical guide pins, although only a single length of power pin is available. Compatibility with the AMP pins should be carefully checked.

- A new power bussing and backplane bracing scheme, forming an integral part of the backplane, is in design. For safety, insulating shrouds will protect all exposed copper. Some form of strain relief system will also be required for the LVDS cables.

Next Phone Conference – 27th February 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman