Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 28th October 2004

Birmingham: **John Garvey, Stephen Hillier, Gilles Mahout, Jürgen Thomas, Dimitrios Typaldos, Peter Watkins**

Heidelberg: **Ralf Achenbach, Paul Hanke, Eike-Erik Kluge, Kambiz Mahboubi, Klaus Schmitt, Hans-Christian Schultz-Coulon**

Mainz: **Stefan Rieke, Uli Schäfer**

QMUL: **Eric Eisenhandler*, Murrough Landon**

RAL: **Bruce Barnett, Tony Gillman, Viraj Perera, Weiming Qian**

***** *at RAL*

1. Birmingham

- Gilles noted that the firmware changes he made to the ROC in the CPM, which will provide separate (asynchronous) clocking of the readout data to the G-links, will be tested next week at RAL.
- The parity-bug fix in the CP FPGA firmware will also be tested next week.
- A total of 6 CPMs should be available for the "backplane stress" tests at RAL next week, although there is a shortage of guide pins and ejector handles for some modules. *[n.b. since the telephone meeting, the necessary spare parts have been obtained.]*
- The latest iteration of the CPM design – CPM1.6 – is ready for manufacture. As the module design is now relatively mature, and the changes are fairly modest, two modules will be made immediately. The main changes relate to the replacement of some PLLs by low-skew devices, and a careful manual re-routing of some of the backplane 160Mbit/s data tracks.

2. Heidelberg

- Paul reported that the complete batch of ASIC production wafers will be delivered to KIP in the next week or so. This will amount to a total of 48 wafers with 190 dies per wafer, to give over 9000 untested dies.
- Four of the FR4 substrate MCMs have been assembled with glob-top encapsulation and will be stress-tested, along with a few of the silicone gel filled MCMs for comparison.
- A single contract is being prepared to define the QA responsibilities of the companies performing the different operations of MCM fabrication (substrate, wire-bonding, etc).
- Assuming that the assembly and QA problems have been fully resolved by then, the PRR for the MCM (and therefore also for the included ASIC) can be scheduled for January 2005.
- An interesting discovery was made at KIP, when the polyimide substrate MCMs from the PPM returned from CERN were re-tested in the test-rig. Initially, the first five devices all appeared to be non-working, but the next four devices tested OK. After that, when the first five were re-tested they were found to be working perfectly. This was believed to be due to the test-rig connector contacts becoming dirty after a long period of disuse (and could even explain some of the MCM problems observed at the ATLAS test-beam).
- The PPM returned from CERN had been identified as having a number of different problems, which are currently being studied at KIP, and many have now been understood and corrected.
- The PHOS4 access problem was caused by incorrect termination of the I2C bus, and by the use of an open-collector drive on the strobe clock line, now changed to a push-pull source. The PHOS4 chips on all 16 MCMs on the PPM can now be accessed and controlled correctly.

- The technique of monitoring the frequency of the PHOS4 reference clock by the “life indicator” detector is ineffective during the power-up and initialisation phase, when unpredictable behaviour is observed. This effect can be eliminated by a subsequent reset of this detector, after which it behaves correctly and monitors the status of the PHOS4 device as intended.
- The configuration and clocking problems seen with the LCD and ReM FPGAs have been fixed, and tested with the home-brew processor but not yet with the Concurrent processor as well.
- The problem with the power management circuits causing module shutdown as the 3.3V supply ramps up has hopefully been solved by adding a choke to suppress the fast current spike seen on module power-up.
- A problem has been seen with I2C access to the TTCrx chip on the TTCdec card, where the I2C address is lost unless a second write operation is performed. Uli noted that he only generates a single write operation to the chip on the JEM TTCdec, and does not see the problem, so this needs further study at KIP.
- The FDR for the PPM should be delayed until ~May 2005, to allow for a probable design iteration of the motherboard. The PRR should be held shortly after this time – probably June 2005.

3. Mainz

- Uli reported that there are three new JEMs in Mainz, plus the one module that was shipped to RAL after use at the ATLAS test-beam.
- Of the three new modules, one has a problem with one of the deskewed clocks, one has a problem with the compact flash memory configuration, and the third module is working correctly.
- The JTAG clocking problems seen earlier in the latest JEMs were partially fixed by the addition of appropriate CR networks to slow the clock edges to reduce sufficiently the effects of reflections. This problem may require a re-design of the clock distribution network on the next iteration of the motherboard.
- There are now sufficient Input daughter-cards for all four JEMs. Although some of the cards were found to have connector shorts, all these have now been fixed. In future production runs, the assembly company will carry out all necessary repairs before delivery.
- The three new JEMs will be sent to RAL next week for further integration and “backplane stress” tests. Extra TTCdec cards will be needed – KIP will loan two from their stock of four.
- There exists a variety of G-link daughter-cards (16-bit and 20-bit versions), all of which are now equipped with optical transceivers.

4. QMUL

- Murrough noted that he had updated the information about our USA15 racks, using the "rack wizard". Details can be found at: http://www.hep.ph.qmul.ac.uk/~landon/atlas/racks/rackwizard.html. Everyone is encouraged to read this and comment on any errors or omissions, before it is submitted to ATLAS Technical Co-ordination.
- Eric reported that the two Wiener air-cooled CP/JEP crates from the scheduled August shipment had finally arrived in Stockholm.

5. RAL

- Viraj reported that there had been some limited progress with testing the 9U ROD module:
- Ian has got the System ACE FPGA configuration logic working, and has also established VME access.

- Adam is setting up a DSS with G-link transmitter daughter-cards to produce optical bitstreams for testing the ROD input channels.
- Weiming noted that he has finished the firmware for many of the input data formats.
- Dave is preparing the firmware to receive the PPM readout data, and discussions may need to be held with Kambiz and Norman to optimise the format of the compressed data at its source.
- The TCM and VMM schematics are finished and will be posted on to the web.
- The four new G-link optical receiver daughter-cards are now ready for testing.
- Bruce reported that all the equipment used in the recent ATLAS test-beam work had arrived back safely from CERN.

Next Phone Conference – Thursday 11th November 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman