Energy-sum and Jet Testing

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Level-1 UK Meeting
Rutherford Lab, 27 April 2004

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Hardware Issues

JEM 0.2 has been written off.
For details see Uli's Post-Mortem report
Casualty of integration battle...

- Readout Controller FPGA not configurable for some time.
- No VME access anymore.
- Module will not be reworked. Concern about internal burned-off tracks. JEM 1 has absolute priority.
- JEM 1 has to be running at RAL in early June. A schedule slip would question JEP running in test beam !
  We have no fallback anymore.
- Work on JemServices and firmware (incl. jet firmware) for JEM 1 need to be finalised.
- Simulation o.k. also for JEM 1
- Merger tests can continue with JEM 0.1 (at RAL, still alive).

Energy-sum Testing: CMM/Sum (1) Setup

Hardware Setup:

DSS/LVDS-source → JEM 0.1 → CMM/Sum Crate Merger and CMM/Sum System Merger → ROD (Neutral) → DSS/S-Link sink

Forced geo-add settings: Merger on left side of crate set to system merger, Merger on right side of crate set to crate-only merger.

Running mode:

Automated checks of the full algorithms using LVDS data feed and readout chain into DSS/S-Link Sink with Kicker. No ROS used then.

Energy-sum Testing: CMM/Sum (2) Results

- Used simple ramp from Dss/JEM-LVDS Generator with simple ramp to find all the DAQ pipeline offsets.
- Bunch crossing number and channel masking now correct.
- Discrepancies on cable parity bit and some overflows are being deal with.
- Parity error problem on some cable inputs.
- Sum-ET thresholds can be correctly set. Changed method of filling of ET-miss LUT not checked yet.
- CTP bits are not identical to simulation.
- More serious sum merging with playback data pending (firmware).

I'm available for conclusion of tests:
Wed 5th May, Thu 6th, Mon 10rd - Fri 14th.

I'll be away afterwards until 1st June.

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Jet Testing: RoI Readout

Setup:

- Remote tests from QMUL, set-up by Bruce. Due to stable hardware setup quite practical.
- Setup: DSS/LVDS source (16 ch., 2 InputFPGAs) into JEM 0.1 with jet-only firmware version provided by Attila. Readout of RoIs into ROD with neutral format firmware.

Results:

- Test patterns: one channel at a time, through all 16 channels: Constant value: RoI stream as expected in the simulation (format as in current spec) apart from known bunch counter reset problem.
- Changing test patterns (ramp up one channel to 255 GeV): Readout offset could not be found. Quite unpredictable results after various offset changes.

→ Algorithm result as expected (for limited number of channels tested).
RoI readout sequencer needs further attention (JEM 1).