Cluster Processor Modules Testing

Uk Meeting, Tuesday the 27th of April 2004

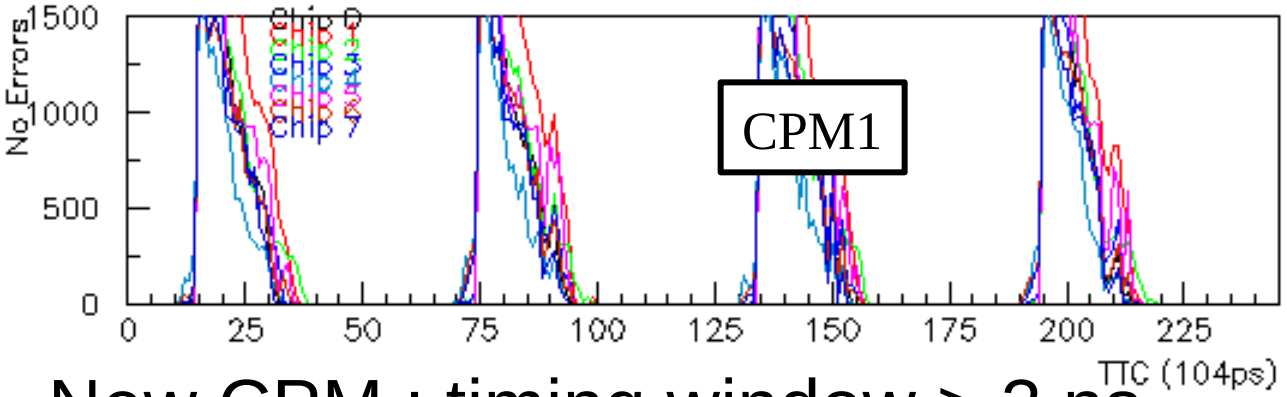
Two New CPM have arrived: CPM1.5

New facilities:

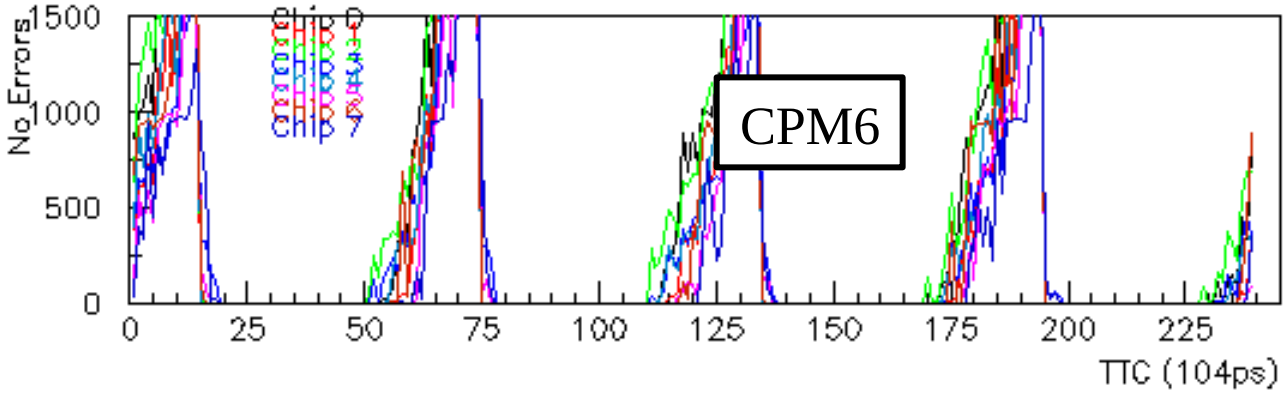
- Extra clock on CP chips
- JTAG access on the front panel
- Test-points on the front panel
- Optical output
- Extra Leds
- Better handles

On-Board Real Time Data Scan

- Old CPM : timing window < 3 ns

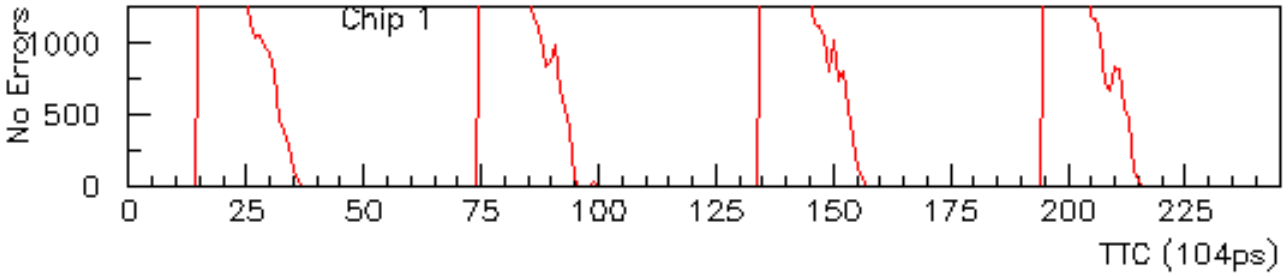


- New CPM : timing window > 3 ns

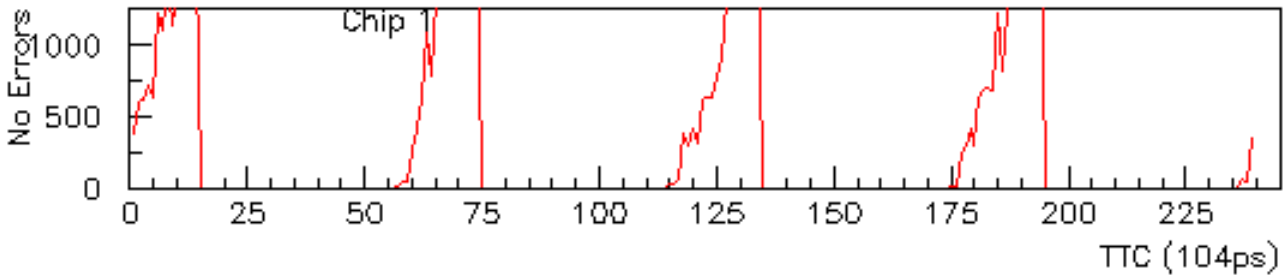


On-Board Real Time Data Scan: per Chip

- Old CPM : timing window < 3.5 ns

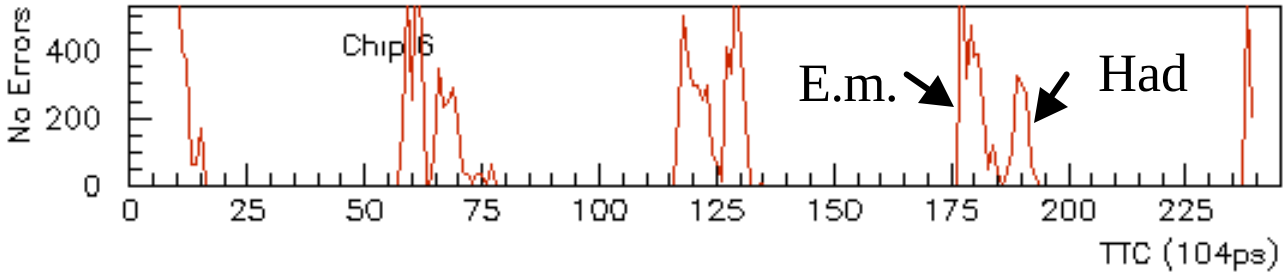


- New CPM : timing window > 4 ns



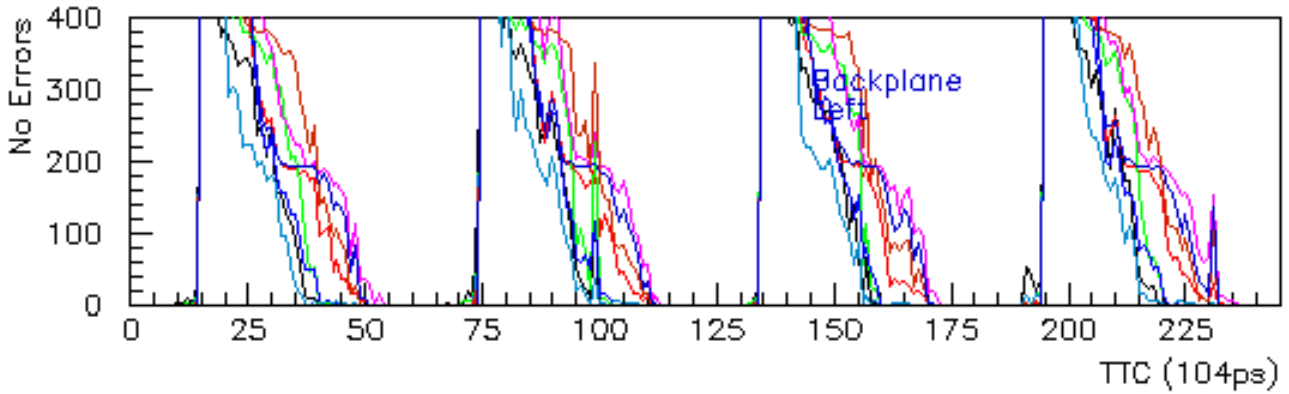
On-Board Real Time Data Scan: per Chip, with self-calibration

- Previous plots:
  - Timings of different pins were put by hand -> all pins have the same timing value
- Plot below:
  - Use calibration of James to set the timing of each individual pins->timing could be different from pin to pin
  - Could see internal delay between group of serialisers, such as between Had and E.m.

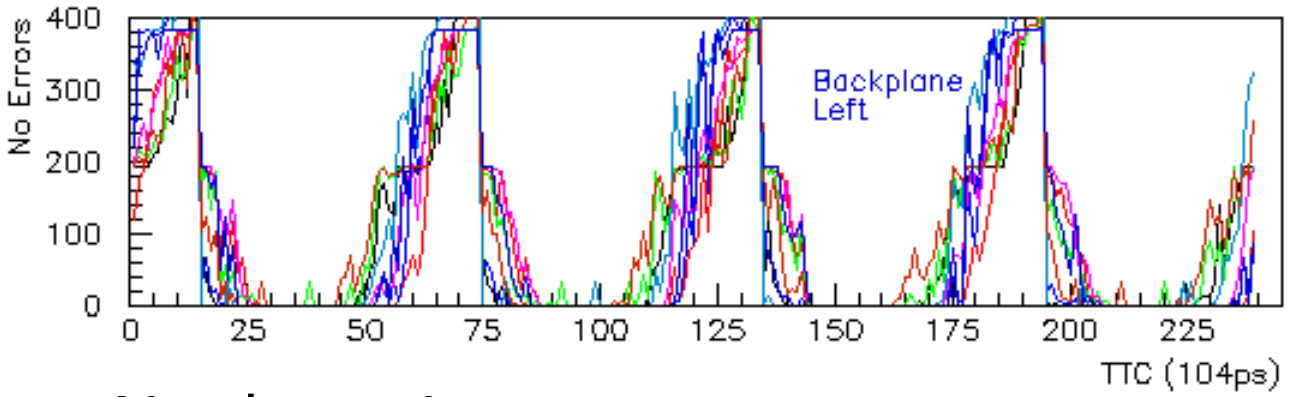


Backplane Real Time Data Scan

- Old CPM : timing window < 1.5 ns



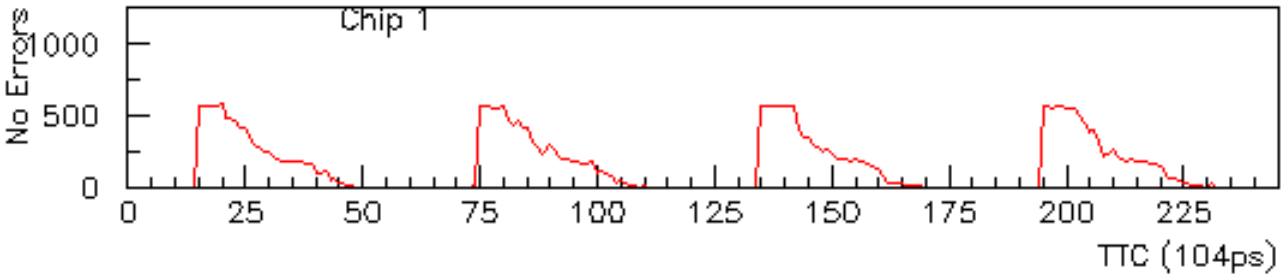
- New CPM : timing window < 1.5 ns



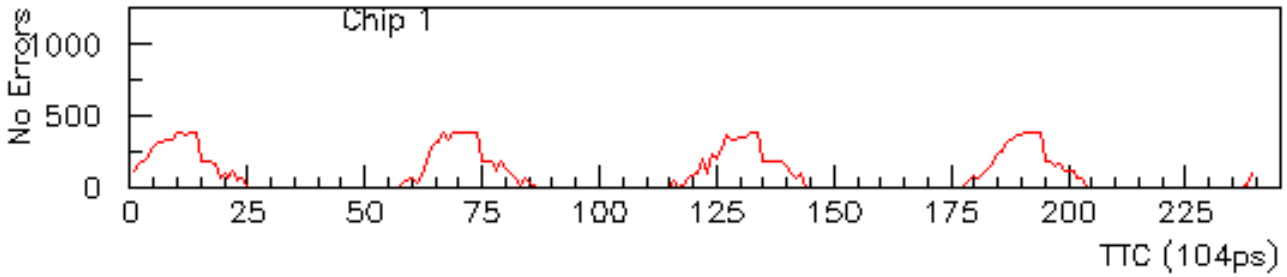
  - No change!
  - Faulty pins on some chips

Backplane Real Time Data Scan: per Chip

- Old CPM : timing window < 2.5 ns



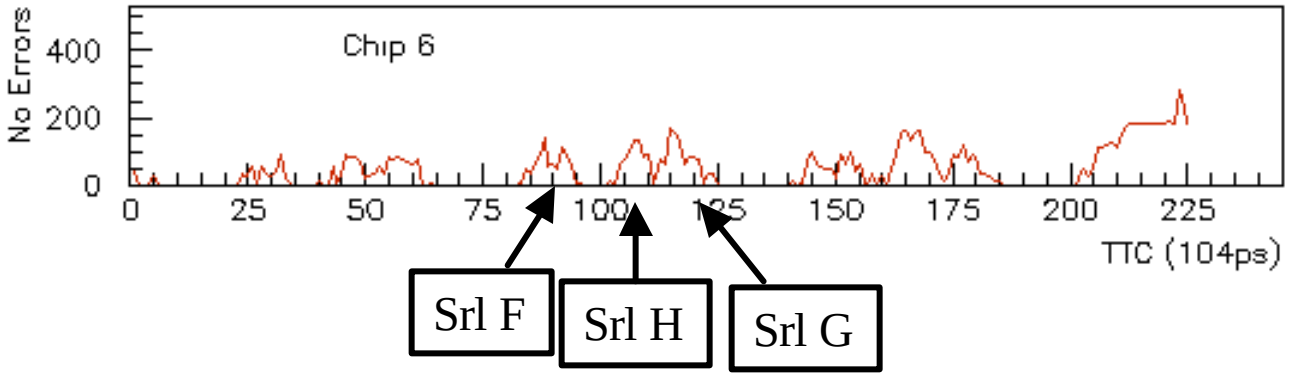
- New CPM : timing window < 3 ns



-> New Cpm has a better timing window due to better signal quality

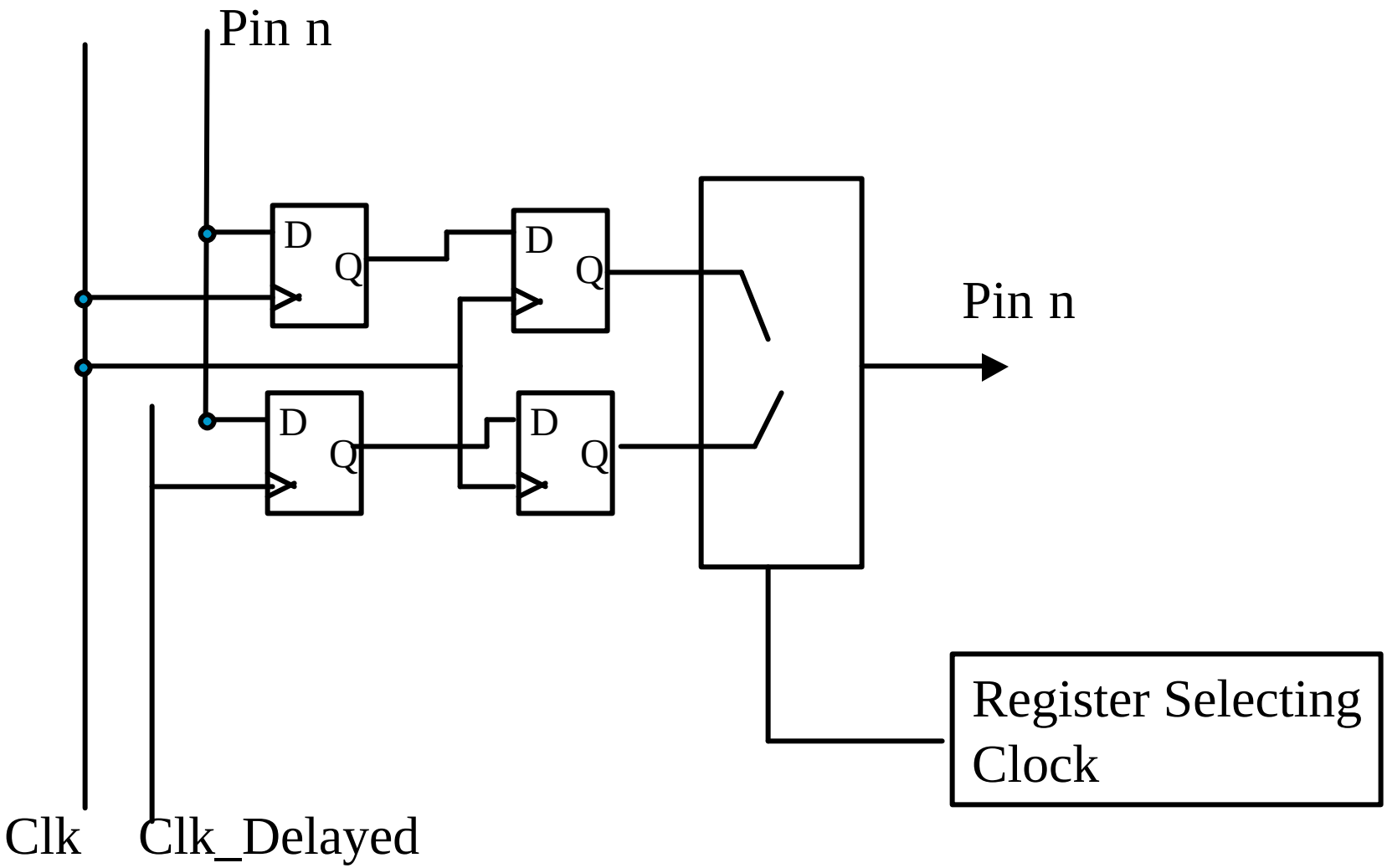
Backplane Real Time Data Scan: per Chip, with self-calibration

- Could see internal delay between serialisers, delays being as big as 2 ns
  - Correspond to different lengths of track between serialisers



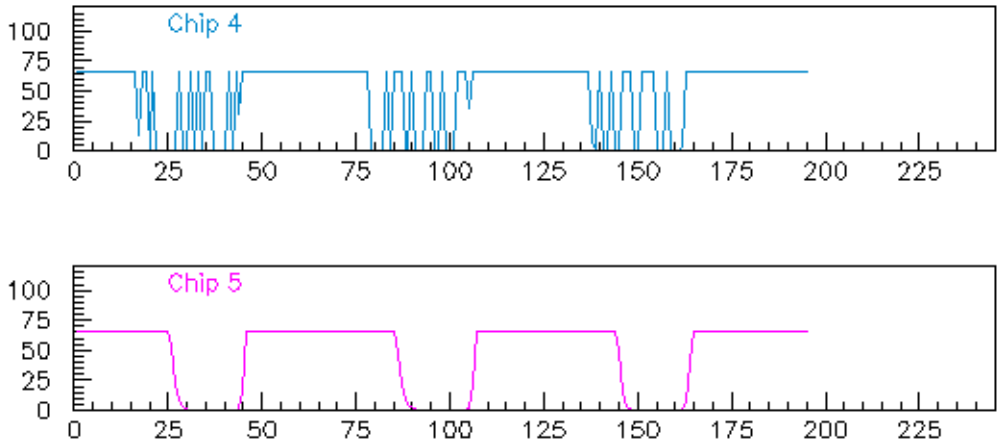
- Thanks to an additional clock, might reduce the spread between serialisers by driving some CP chips pins coming from a serialiser with a different clock
  - Need different F/Ws from CP chip to CP chip or
  - Generic F/W with a register setting which clock to be used for the CP chips pins coming from the backplane

CP chips modification



New CPM : Algorithm test

- Test with algorithm is working normally, on On-Board data
- Backplane data instable due to some pins misbehaving
- Lot of parity errors observed on those faulty Pins



- At least 2 CP chips on CPM6 have faulty pins
  - Same location
  - Signal has been re-routed to testpoint: looks OK
  - Still need some investigation

CPM1.5: Readout

- No deterministic jitter observed!
- Readout working correctly at B'ham
  - Need to shift the offset by 1
- New CPM integrated successfully at RAL
  - Min. dead-time between DAV has to be increased
  - Work with old offsets
  - Optical output tested successfully

Second CPM1.5 (CPM7)

- Readout and On-board signals are OK
- More CP chips with problems of back-plane pins I/O

Next Integration Test at Ral

- Testing parity behavior with new serialiser F/W from Tamsin
  - Implement similar modification in CP chip code
- Testing parity/Bcmux bits swapping to accommodate PPM format
- Testing CTP output: GIO rx card
  - Re-measure latency