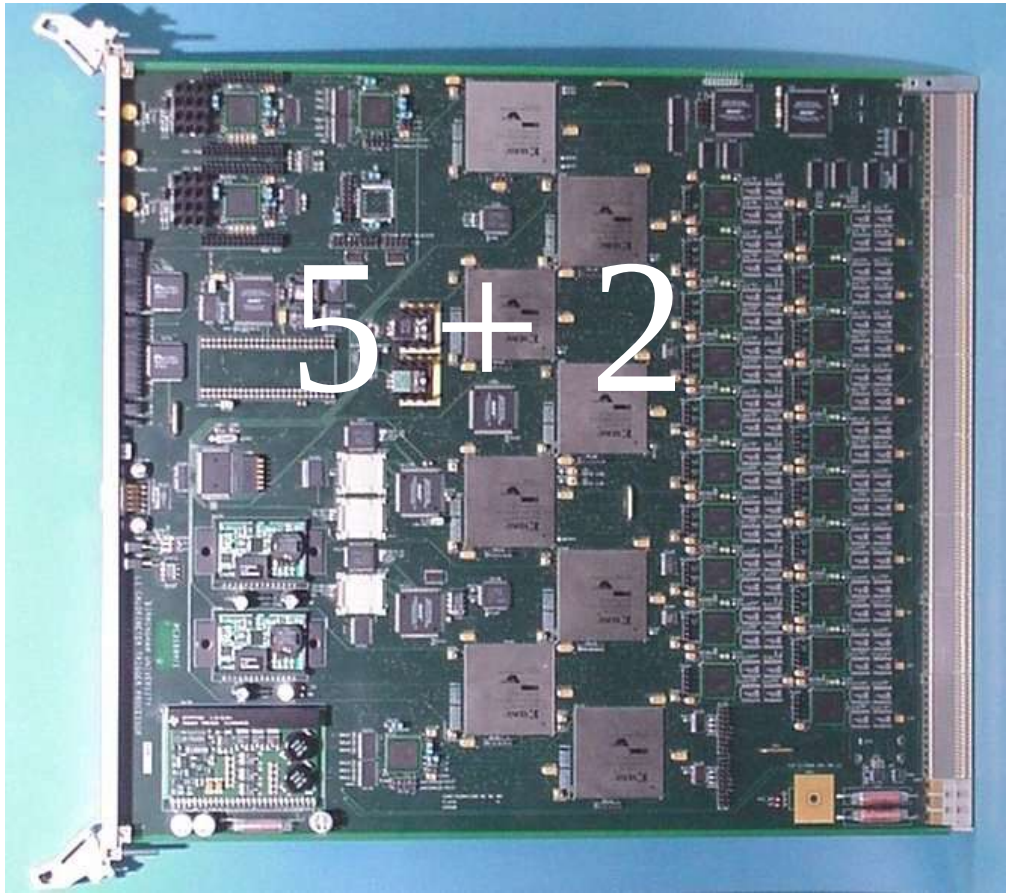
CPM Prototype Hardware Status

Hardware Status

- PCB/1 and PCB/2
- Layout
- Timescales
- Summary



R. Staley

THE UNIVERSITY
OF BIRMINGHAM

Hardware Status

PCB/1

CPM#1 - Assembled and fully working
CPM #2 - Assembled, but assembly defects with 4 CP FPGAs .
CPM #3 - Sent to PCB Assembly Company for Termal Profile.
CPM #4 & #5 - Assembled and fully working.

PCB/2

CPM #6 & #7 - Assembled, pass JTAG and undergoing tests…

New CPMs (#6 & #7)

Design Checks…

- VME interface running
- FPGAs Configure
- TTCdec running with no L1A induced Jitter
- TTCrx I2C working
- Some CP Chips reading '0' on few inputs

  investigating… (new Vref connection ?)

Backplane Signal Quality much improved but there are timing issues:

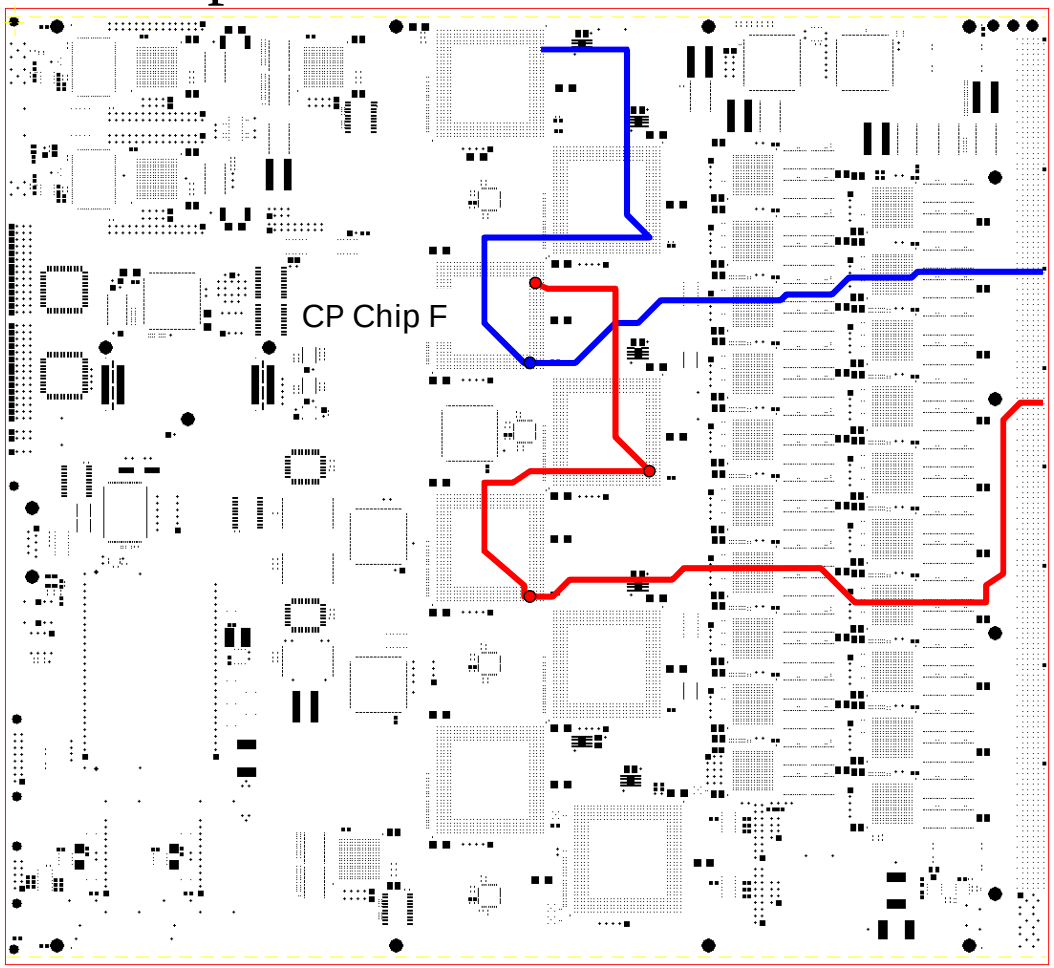
- New PLLs have much more jitter than expected

  Investigate an alternative device. Test PCB.

- Time distribution of backplane inputs (all together) too wide.

  Add extra clock to CP Chip. PCB option + Firmware change.
  Examine layout - identify tracks too long / too short.

Why is data arriving with such a large timing spread?
CP Chips are bussed.



G_IPE<4> to CP chip F = 210mm

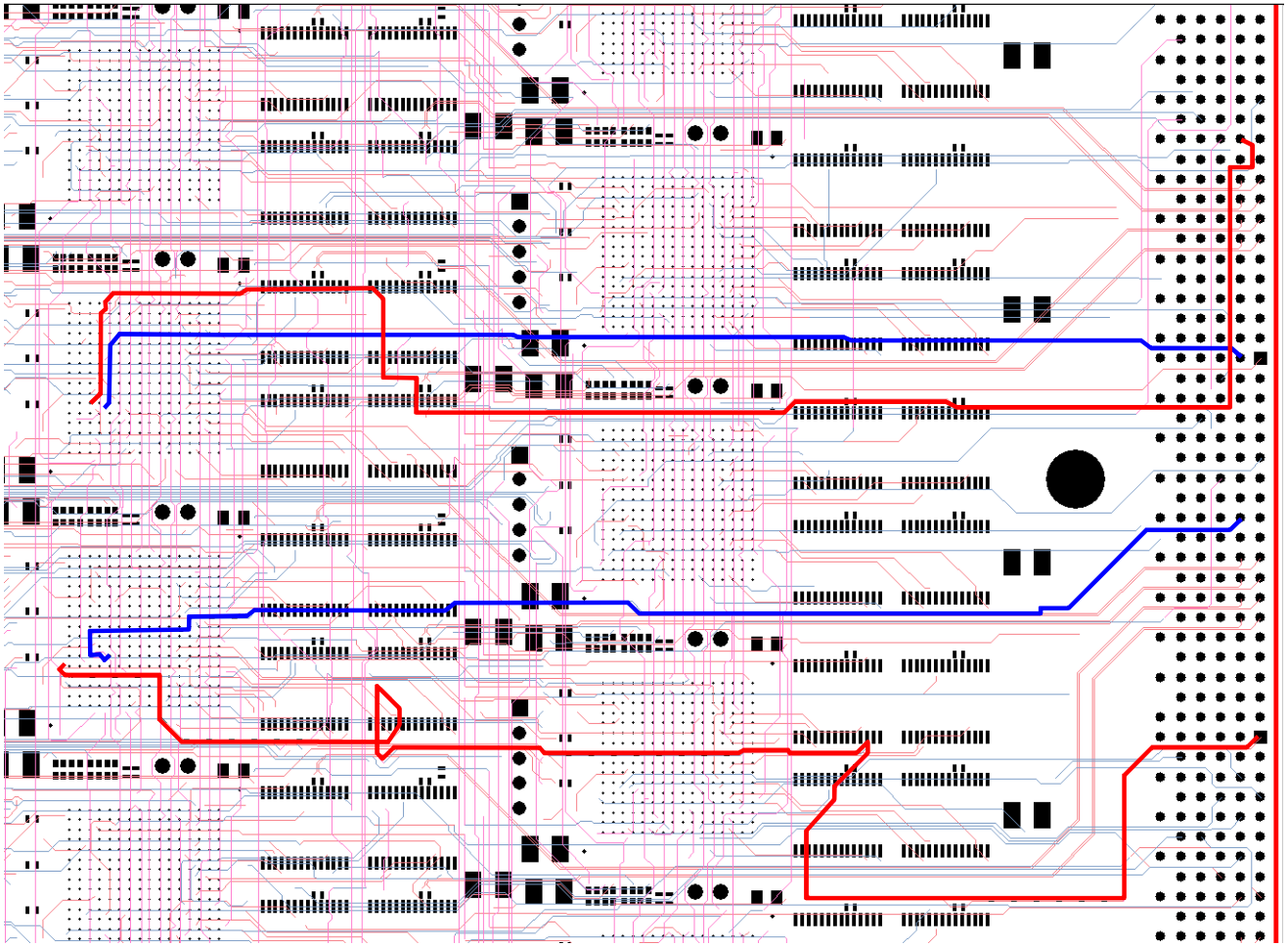
E_IPE<4> to CP chip F = 523mm

Path difference = 313mm = 2.3ns

R. Staley

THE UNIVERSITY OF BIRMINGHAM

… and some outgoing tracks are still auto-routed:



F_DQE0 = 168mm
5 vias

Path difference = 47 mm
= 338ps

F_DQE2 = 121mm
1 via

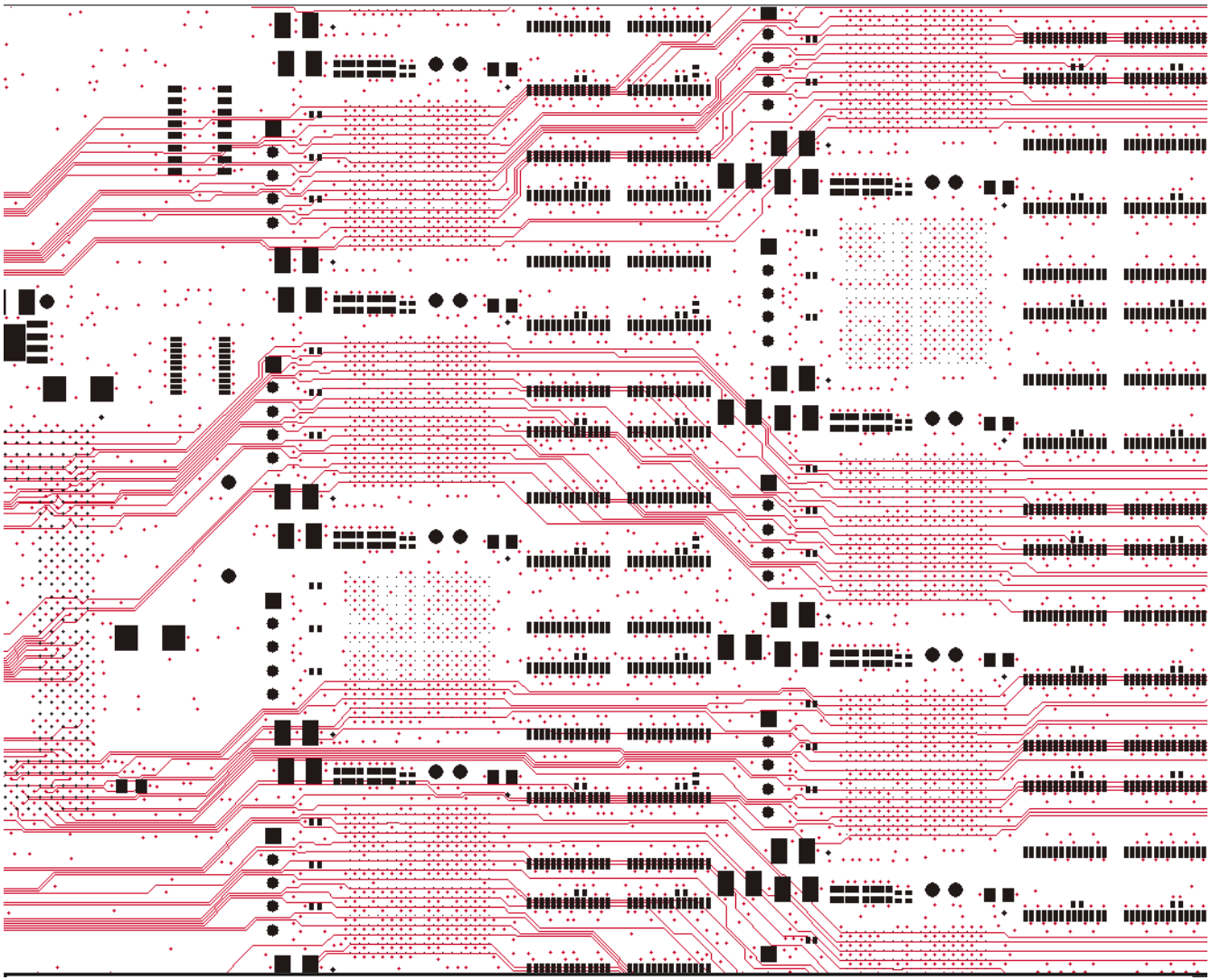
E_DQE2 = 126mm
3 vias

Path difference = 54 mm
= 388ps

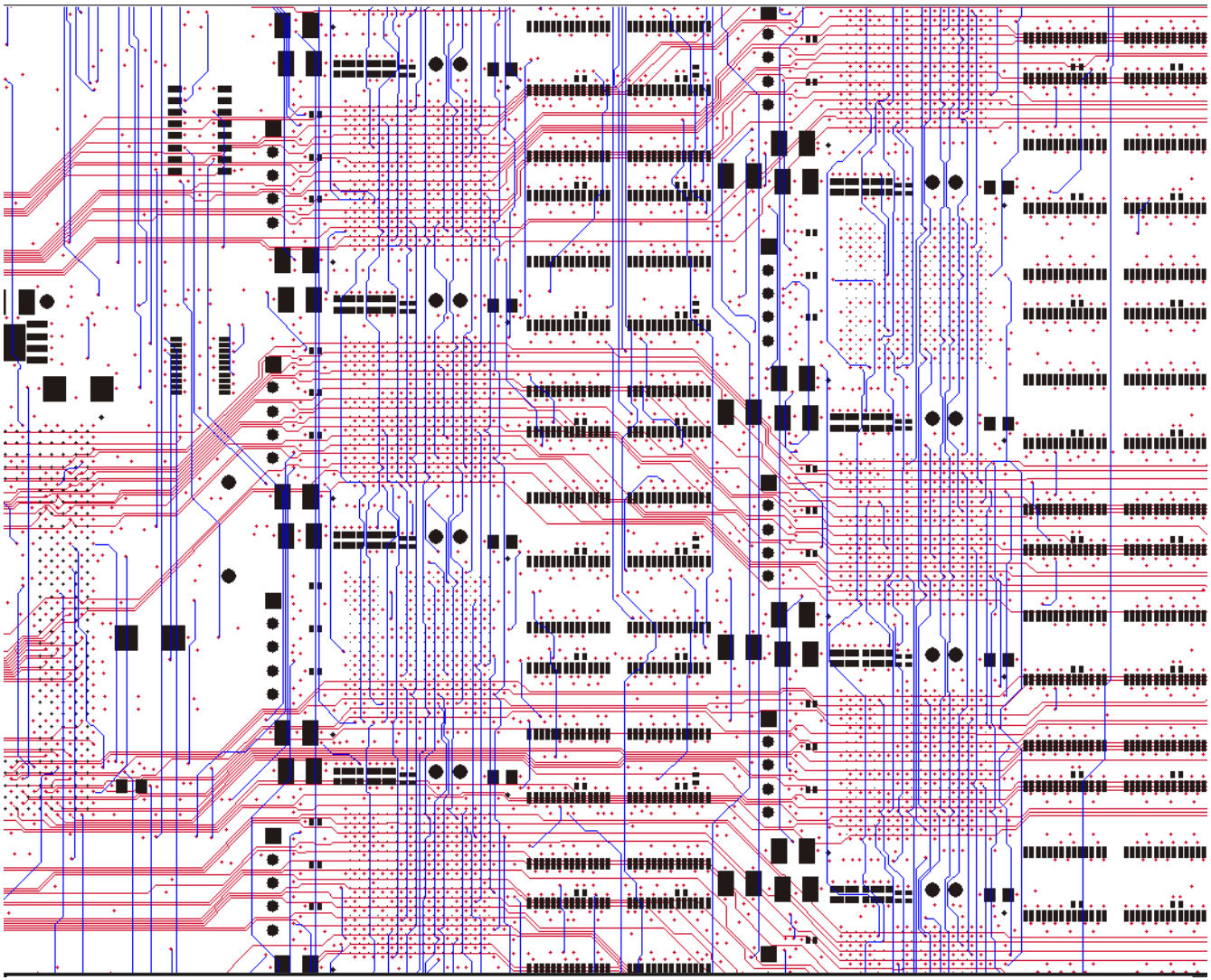
E_DQE3 = 180mm
7 vias

How complex is the PCB?

R. Staley



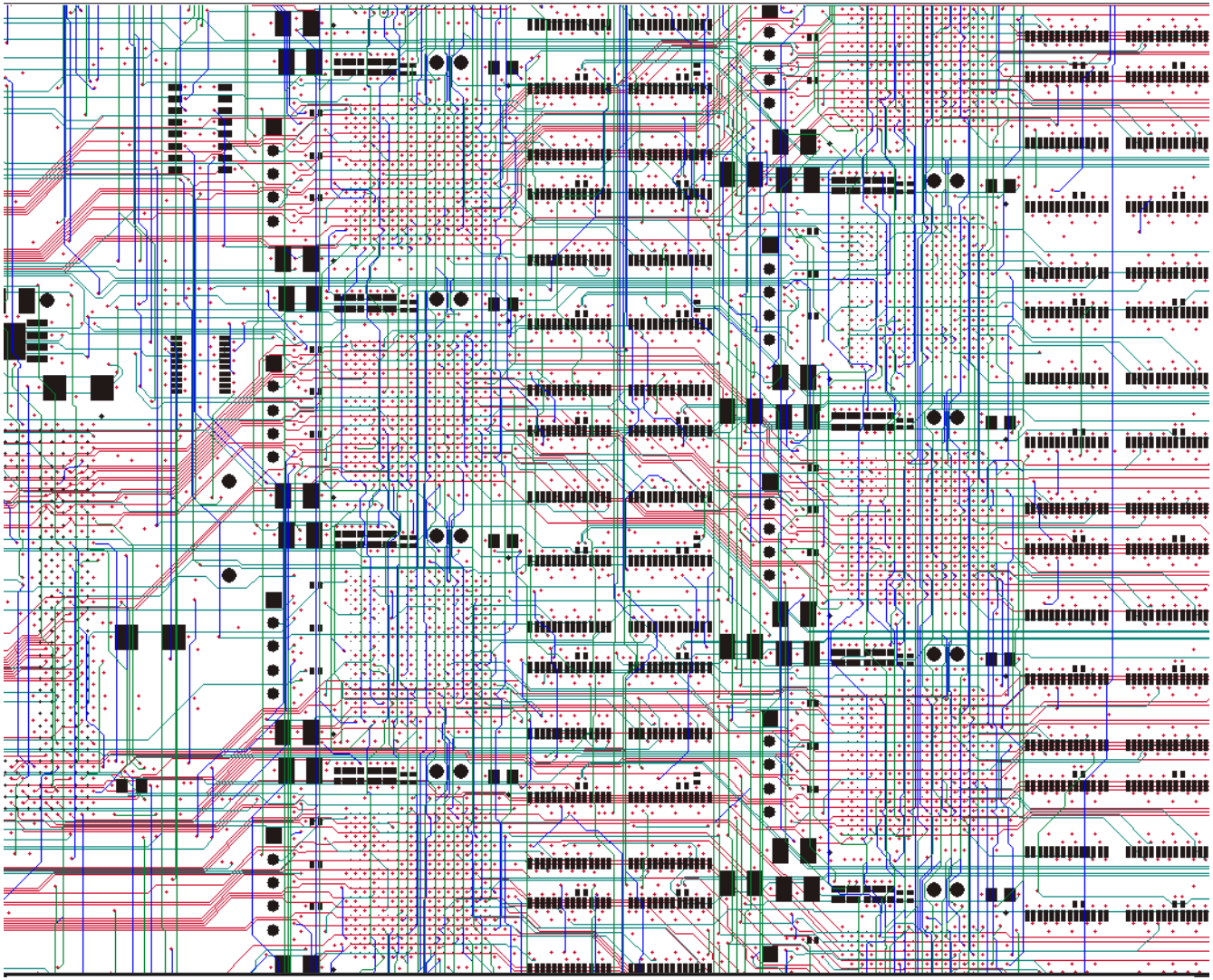
Layer1



Layers 1 & 2

R. Staley

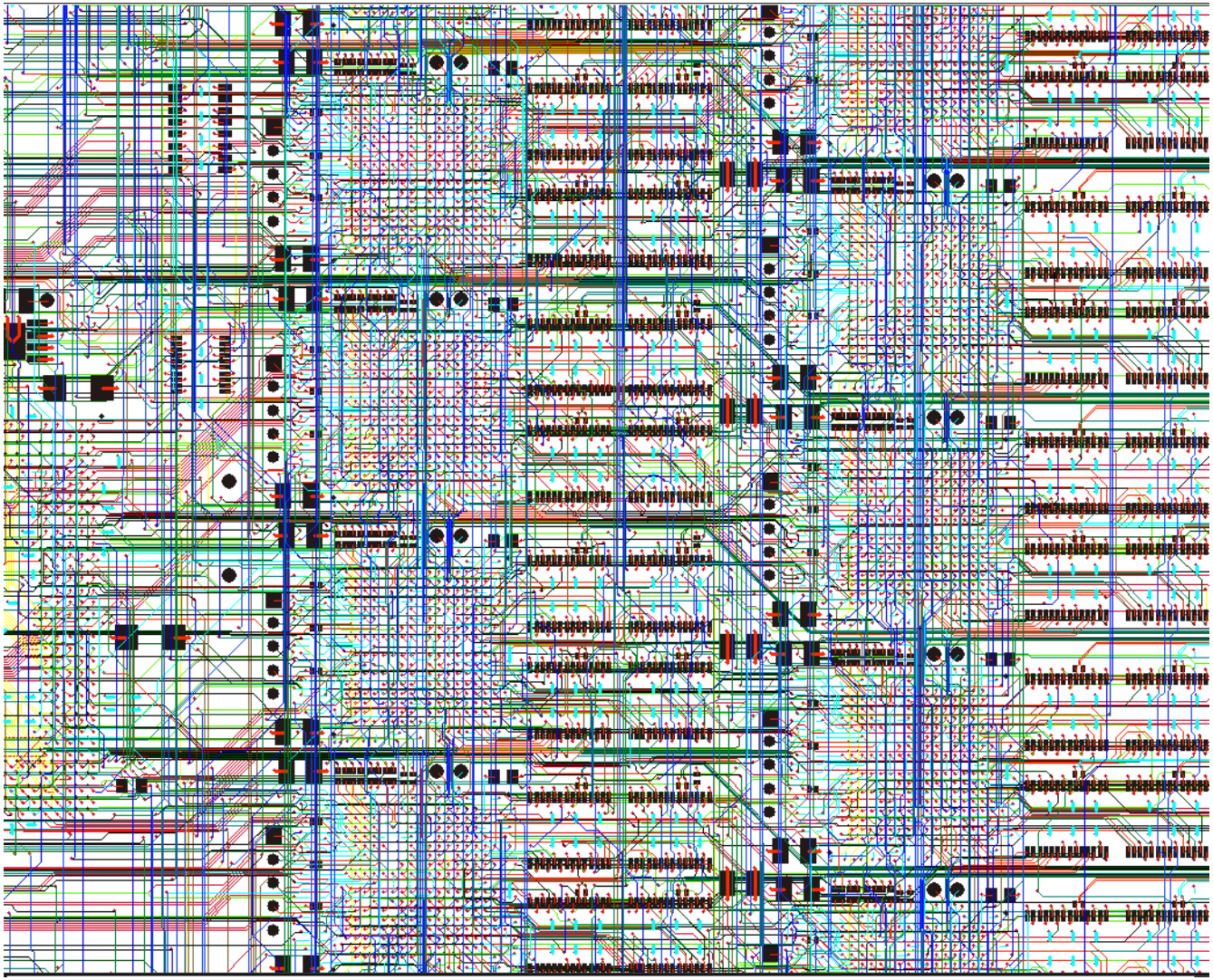
THE UNIVERSITY
OF BIRMINGHAM



Layers 1 ,2 , 3 & 4

R. Staley

THE UNIVERSITY
OF BIRMINGHAM



All Layers

R. Staley

THE UNIVERSITY
OF BIRMINGHAM

Reminder

CPM/1 was a "prototype pcb designed to production specification"

CPM/2 is CPM/1 with 'minor' changes.

- Mechanical bracing
- CP chip calibration removed
- Clock distribution tighter
- Signal layout improved.

CPM/1 to CPM/2 took 2 YEARS!

Summary

- New CPMs (/2) pass JTAG. Good Assembly DDi!
- Control functions working
- Backplane Timing Margins poor. Extra clock for CP Chip