Minutes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 27 Oct. 2005

Birmingham: Steve Hillier, Gilles Mahout, Richard Staley
Heidelberg: Victor Andrei, Florian Föhlisch, Paul Hanke, Kambiz Mahboubi, Karlheinz Meier, Frederik Rühr, Klaus Schmidt, Hans-Christian Schultz-Coulon, Pavel Weber
Mainz: Uli Schäfer, Rainer Stamen (both at RAL)
Queen Mary: Paolo Adragna, Eric Eisenhandler (at RAL; chair and minutes), Murrough Landon
RAL: Bruce Barnett, Richard Booth, Viraj Perera, Weiming Qian
Stockholm: Christian Bohm, Sten Hellman, Sam Silverstein

Birmingham
Gilles reported that the two new pre-production CPMs have arrived and are working well. Minor faults were found and fixed during JTAG testing at RAL and on arrival at Birmingham. LVDS inputs, CP-chip input window, readout, and real-time path to CMM all seem fine. The VME problem on earlier versions has now been fixed. Timing windows are 2.5 ns wide, but settings for that are board-dependent; if not individually adjusted than the windows are 2.2–2.3 ns wide.

Before making the next 10 modules it is desirable to integrate with the PPM inputs and the ROD. This will be tried at RAL within the next week or so.

Richard said that the RPPPs have gone out for price quotations. The Patch Panel Tester is being completed and will be tested next week.

Gilles would like some broken backplane pins repaired. Sam said Weiming could do that – the repair kit is at RAL (despite some confusion).

Heidelberg
The PPM was tested with TileCal signals again at CERN last week. Kambiz reported a very successful effort by himself, Florian and Frederik, together with Norman and Murrough and with the assistance of Paulo da Silva and Oleg Solovyanov (TileCal) and Chaouki Boulahouache (LAr, Receivers). In addition to gathering a lot of data on pulse shapes, behaviour, and initial calibration, first via direct connection and then via Receiver, a lot of progress was made on automating and speeding up the software. A large and varied set of plots is available at:
http://www.kip.uni-heidelberg.de/atlas/tests/tile1_amplitude_calib.html

Mainz
Uli said that he and Rainer are now testing JEM 1.2 at RAL. The two FPGAs had been accidentally swapped in manufacture, and after re-work it seemed that one ball on the jet FPGA is not connected. A temporary rearrangement needs Attila to fix the firmware, which he said would be done by the end of the meeting. Otherwise things are going fairly well.

Queen Mary
Eric said that the agenda for the CERN joint meeting is starting to take shape, but since the agenda system doesn't have a nice way to sketch in an outline it will be early next week before the details will be revealed.

RAL
Viraj said that the two pre-production CMMs have now been ordered, but a delay in delivery of the 3M connectors used for crate-to-system and and system-to-CTP cables means the modules will not be available until early December. Ian has the modified firmware ready.

The new ROD prototypes have also been ordered, but there is a delay to get the dual-port RAMs for the monitor FPGA. As that FPGA is not yet in use, one possibility is to leave the RAMs off for now in order to get the modules.

The VMM design was checked by Uli, and is now out for price quotations.

The TCM has to be reviewed (FDR) before it can make much further progress.

Weiming said that outstanding changes to the TTCdec card are now implemented, except for the question of the PLL on the output. There are conflicting requests: Heidelberg says the PLL causes jitter that compromises their LVDS outputs, while Richard says the CPM needs it to compensate for the timing drift with temperature, and Uli relies on it too. Although we would much prefer to have only one type of card, and Weiming will try again to think of a way to do that, that may not be feasible. The suggestion of jumpers is probably no better than having two types of card, especially if the two types can be made mechanically incompatible in order to avoid using the wrong one.

Bruce said that short tests with the ROD using native JEM readout formats had been done. Next week Kambiz will come to RAL to do more PreProcessor Module testing.

Stockholm

Sam said that the decision on who will manufacture the backplane has now been made and the order can be placed next week. Delivery will take 7 weeks.

The high-current power pins needed, which have just been made obsolete, have been specially ordered and will be delivered in 10 weeks.

Sam would like a CMM rear-transition module in order to sort out the support mechanics.

Sten said that LVDS cables have been flowing in, and they now have 1100. They look correct, so 30 will be shipped to Birmingham today or tomorrow for testing.

The first 1 km of analogue TileCal cable from Sweden is finally en route to CERN; the firm is already making the other 4 km at their own risk.