Preliminary Design Review of Data Source-Sink System
(ATLAS Level-1 Calorimeter Trigger)

Introduction

The PDR for the DSS system took place during February 1999. Its purpose was to assess the functionality, features and feasibility of the DSS test system as it would be applied to the evaluation of different components of the ATLAS level-1 calorimeter trigger system, during both the prototype and production phases. The review was conducted largely by e-mail, with a final series of meetings with the designers during which the collated list of comments was discussed.

It was intended that the review panel should assess the system specifications from several different aspects, so the reviewers were chosen for having expertise in areas of electronics and system engineering, data acquisition and software. The panel consisted of:

Tony Gillman (RAL)

Paul Hanke (Heidelberg)

Viraj Perera (RAL)

Uli Schaefer (Mainz)

Richard Staley (Birmingham)

Scott Talbot (Birmingham)

Comments from others in the level-1 calorimeter trigger community were also received, and were channelled via these people.

The designers made available three sets of specification documents to the review panel, covering the following sub-systems:

a) Data Source and Sink Module Specifications
b) LVDS Source and Sink CMC Daughter Boards Specifications
c) G-Link Daughter Boards Specifications

All documentation was available on the Web, at:

http://hepnts1.rl.ac.uk/atlas-l1/Modules/Modules.html

General comments

The panel commented that the largest section of the documentation, which was concerned with the DSS module (mother-board) specifications, was slightly confusing and ambiguous in places. To a large extent this reflected the difficulty of clearly and concisely describing the variety of applications for this module, but it was strongly felt that the documentation would benefit from some careful revision. The documentation describing the specifications for the LVDS and G-link daughter boards was considered to be sufficiently clearly written, although the level of detail given for the LVDS daughter boards was thought to be somewhat sparse. For the system as a whole, however, sufficient detail was supplied (or clarified in discussion) to enable the panel to make an informed assessment of the proposed designs.

The reviewers were generally favourably impressed that the proposed system would have considerable power and flexibility to act as the major test facility for several parts of the level-1 calorimeter trigger system. The data-flow architecture and the generous use of re-

configurable FPGAs for data generation and verification was felt to be soundly based, allowing adequate freedom for future applications. No "show-stoppers" were found, and they agreed that the system was feasible and of an appropriate level of ambition.

Specific comments

A large number of points were raised by the review panel, only the more important of which will be summarised here. The majority of the comments related to the specifications of the DSS module mother-board, in which resides most of the functionality of the system.

a) DSS mother-board

One major area which was addressed was the proposed programming model, and the reviewers recommended several areas where improvements could be made, with the opportunity to create a more user-friendly software environment. The inclusion of programming model guidelines was welcomed, and the hope was expressed that other module designers would adopt a similar approach.

In general, it was recommended that the address map be revised to create a much simpler structure, encouraging fewer programming bugs. It was also recommended that the mother-board and daughter-board IDs should be held in separate registers rather than being combined, and in a similar vein it was considered that there should be a separate class of control register for all pulsed signals, such as resets. (It was noted that a uniform policy for all module designs would be very desirable.) The bit-field groupings in some registers (e.g. the mother-board control register) were considered non-optimum from software considerations and should be re-ordered into a cleaner structure.

When considering the programming model relating to the FPGAs it was noted that only one pair of registers had been provided to monitor the data words where transmission errors occur, together with their associated addresses, whereas each FPGA requires its own pair. It was also recommended that extra registers be provided to hold the configuration code version for the FPGAs. It was considered that an alternative path for re-configuring the FPGAs, using the VME-bus, should be provided if it were possible without adding significant complication. It was also noted that the single-bit indication that all FPGAs had correctly loaded should be the AND (not OR) of the individual PROM_DONE signals.

Finally, the designers were also encouraged to find a fail-safe way of indicating to the software the absence or presence of an S-link board, and its type (source or sink).

In the area of electronics, one major issue concerned the asymmetric series-parallel technique proposed to terminate the large number of controlled-impedance traces conveying 40 MHz data signals between mother-board and daughter-boards via the three connectors. The review panel suggested a simpler symmetric scheme, whereby purely series terminations were used. This would require much lower drive currents from the mother-board FPGAs, with consequently reduced ground-bounce, etc. (As it has subsequently been found necessary to reduce the board trace impedances from 100 ohms to 75 ohms in order to accommodate standard pcb thicknesses this recommendation now carries even more weight.)

The panel also urged close and frequent interaction between the mother-board and daughter-board designers to minimise the potential for errors at the physical interface. It was considered essential that a consistent terminology be used to define the inter-board connector pins in all three sets of specification documents.

b) LVDS daughter-boards

The panel felt that more detail should be included in this specification document, to match that provided for the DSS mother-board. In particular, some further elaboration of how the boards will be used for evaluating the LVDS links should be included. The panel also encouraged the designer to ensure that the grounding scheme for the cables and connectors carrying the 480 Mbit/s LVDS bitstream signals is fully thought out, and that suitable cable is available.

c) G-link daughter-boards

During the review process it was realised that the G-link receiver board could probably be used as a two-channel diagnostic device for the Heidelberg MCM, mounting on their mother-board. Only small modifications to the existing specifications would be needed (e.g. the provision of a programmable control bit to select 16-bit or 20-bit operating mode) so the review panel recommended that these be made (with the exception of changing to SMA input connectors). A further recommendation was the provision of separate programmable control lines for the cable equalisation (EQEN) inputs for each G-link receiver.

The panel expressed some concern about the cooling problems associated with four G-link receivers, with a total dissipation of almost 10 W. It was recommended that these devices be mounted on the daughter-board side facing away from the mother-board, in order to minimise the air-flow impedance, but at the expense of making the overall DSS module double-width.

It was again stressed that the overall grounding scheme for the high-speed bitstream signals, and their associated cables and connectors, should be carefully considered.