ATLAS Level-1 Calorimeter Trigger

LVDS to NIM Module (LTN)

A module to convert CMM LVDS outputs into NIM levels for local triggering use.

Design Specification

Version: draft 3
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Table of Contents

Document History

Version	Main changes
Draft1.	Discussion Document.
Draft2.	Implementation details added.
Draft3.	Complex Dead-time Number now adjustable.

Updates to this document “LTN_Specification.pdf” and other information can be found at:

http://www.ep.ph.bham.ac.uk/user/staley/LTN/

1 Introduction

This document describes the specification for a proposed LVDS to NIM converter.

1.1 Overview

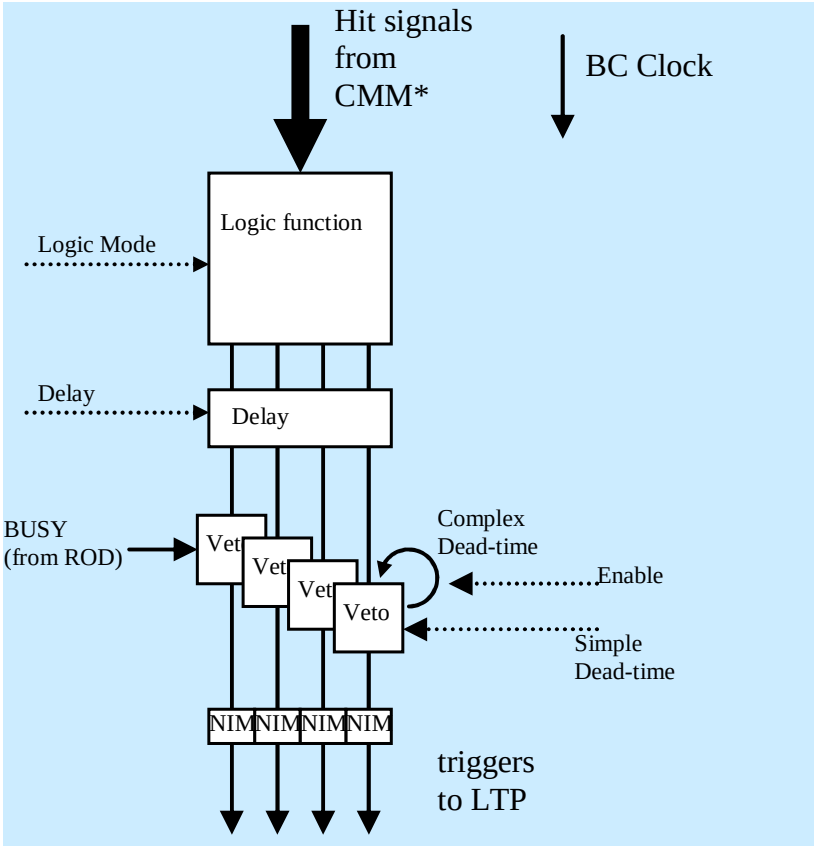
For commissioning of the L1 Calo Trigger Processor it is useful to self trigger the local system without involving the CTP. This module will translate the LVDS signals from a CMM into NIM level trigger signals required by the LTP/TTCvi sub-system, while performing some simple logic and veto functions.

The outputs from a CMM are defined by the type of crate this module is used in, so the LTN's design must take account of this.

2 Requirements

- Receive 32* LVDS signals and clock from CMM via 68 way MDR type cable connector. Parity of input data will be checked and errors indicated.
- Output 12 NIM signals as a selection or as simple logic functions of these inputs
- Output 1 NIM version of clock input
- Input logic functions:
    - Individual inputs passed through 0 to n-1
    - Individual inputs passed through n to 2n-1
    - Logic OR of groups of 3 bits (for CP hits) i.e. non-zero count.
    - Logic OR of groups of 4 bits (for energies)
- Provide adjustable coarse delay to all output signals
    - Delay of N BC periods (N = 1 to 15)
- Provide veto on each output signal
    - Dead-time of N BC periods (25ns) to all outputs (N = 1 to 50)
- Provide complex dead-time veto on each output signal
    - Allow maximum of 8 triggers within 80us
- Receive BUSY signal from ROD
    - CTP 'TTL' signal but reconfigurable to accept NIM signal.

*There are actually 33 LVDS channels on the cable, including a clock signal and a parity bit



Block Diagram showing order of functions.

3 Implementation

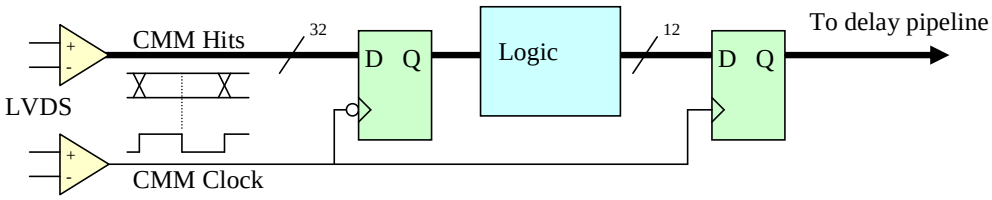
Constructed to fit into a 6U VME crate, but will not have a VME interface. The module will only draw power from the backplane slot.

The module will use a single FPGA, an Altera Cyclone II FPGA EP2C5, to perform all the logical and delay functions. The design uses pipelines for the delay and deadtime functions and requires a 25ns clock from the CMM. Incoming signals are sampled by the falling edge of the CMM clock, outgoing signals are clocked out on the rising edge.

The Incoming LVDS signals are received directly by the FPGA, but the outputs of the FPGA need translation to NIM levels. The translation will be done using a number of small daughter cards, one per NIM output. This gives extra flexibility to the module as it may be easily adapted to output other logic standards, or even to receive extra signals back into the FPGA, by changing the daughter card.

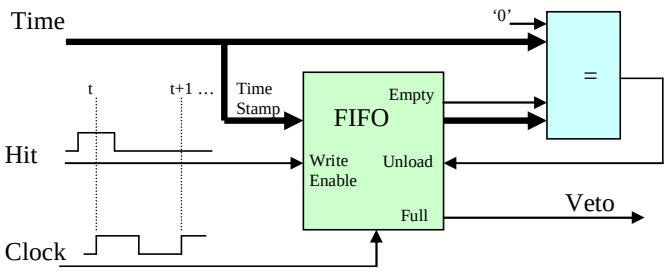
The grouping of the inputs from each type of CMM are shown by the table in Appendix A.

3.1 Input Stage



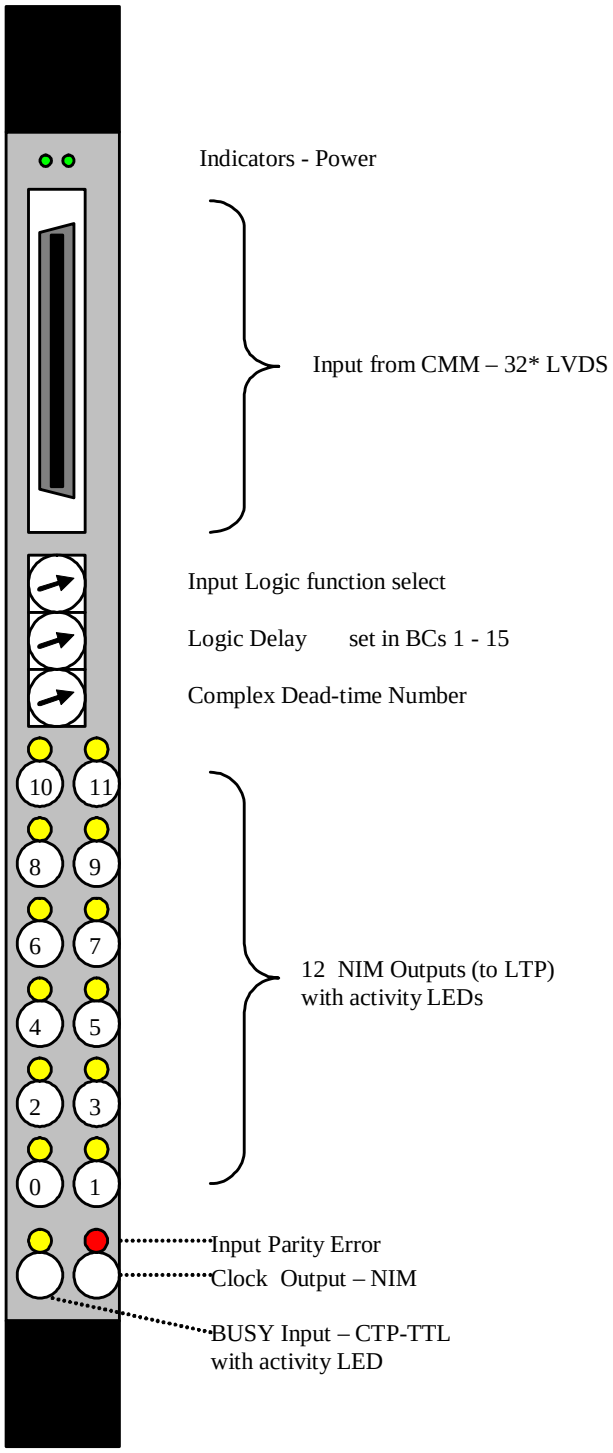
3.2 Complex Dead-time (Leaky Bucket algorithm)

This algorithm will apply to each output individually. A counter generates a time-stamp value for each hit which will be written into a FIFO memory. Once the earliest time-stamp stored in the FIFO matches the wrapped-around time it is unloaded from the FIFO. The Veto will be active Whenever the FIFO is full, the Veto will be active, and the FIFO will not take anymore time-stamps.

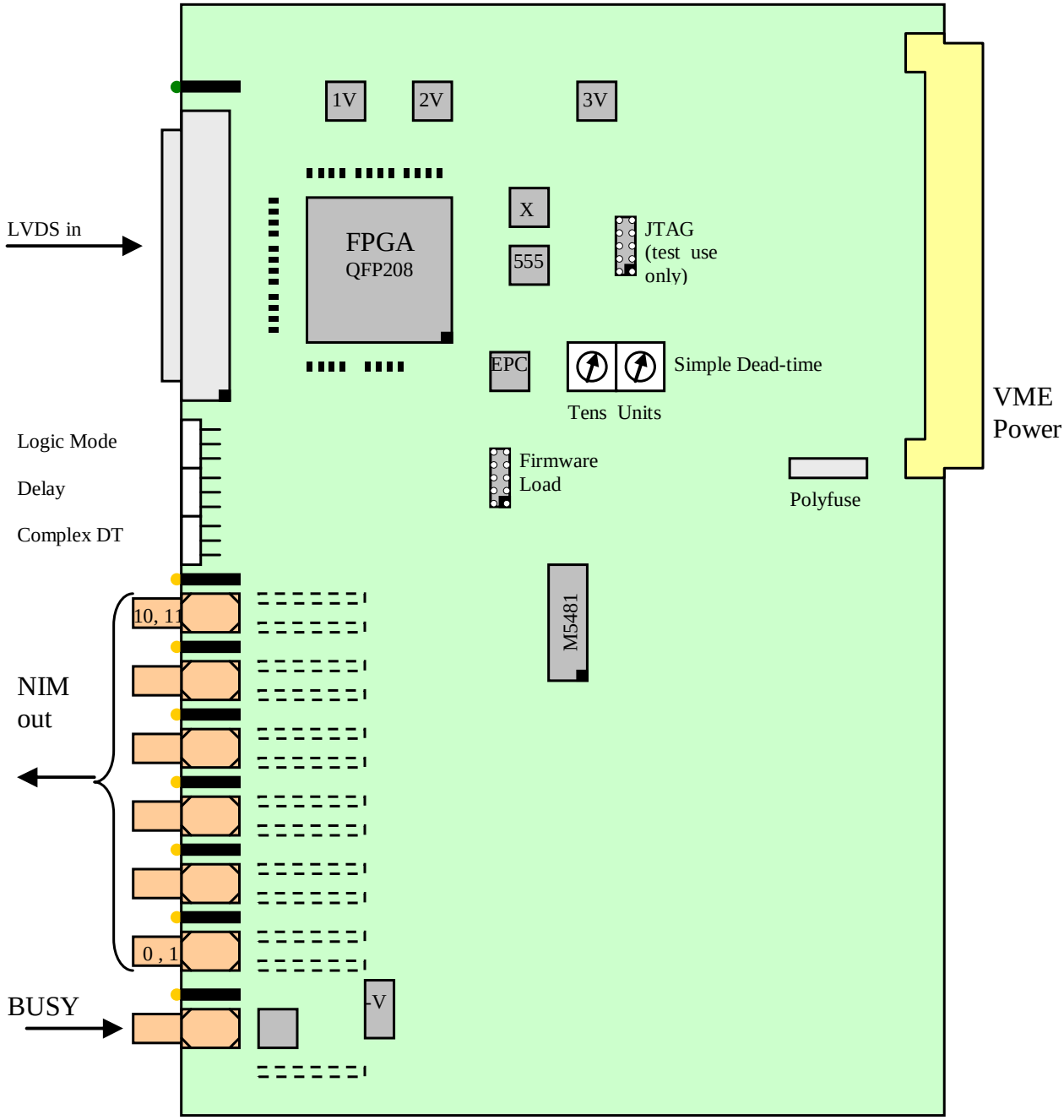


The counter has a modulus equal to the dead-time in BCs (3200 = 80μs), and the FIFO depth defines the number of hits allowed within this time. The FIFO depth may be set to values from 1 to 8.

3.3 Front Panel



3.4 Module Layout



4 Project Management

4.1 Deliverables

- Specification (this document).
- 1 prototype LTN followed by 6 production modules.
- Firmware for programmable logic.
- Design documentation (schematics, layout information, component data-sheets etc.)

4.2 Personnel

The LTN is designed at Birmingham University to specifications set by members of the Level-1 Calorimeter Trigger Collaboration.

4.3 Design and Verification

- PCB Schematics and layout using OrCAD 9.2 Software.
- FPGA design and verification using Altera Quartus 7.2 Software

4.4 Manufacturing

The module is based on a 4 (or 6 layer) PCB manufactured by PCB-Pool.

The modules will be assembled by technicians at Birmingham University.
1 prototype module will be made and tested before the remaining ones are produced.

4.5 Test

The modules will go through a number of stages before being released to CERN:

- Using pulse generator and oscilloscope to check signal levels and basic operation.
- Module will be placed into Birmingham test rig and tested with signals from CMM.

4.6 Costs

	NRE costs	Cost each in UKP
1 PCB - 4 Layer prototype / 8 day	£22 silk screen stencil	£245
6 PCBs - 4 Layer production / 8 day	£22 silk screen stencil	£148
Components	-	£277
Assembly	-	Birmingham Technicians

Costs given above exclude VAT.

Appendix A CMM Front-panel connector

Pinout for different CMM versions

Pin Pair	CP sk#1	JET sk#1	JET sk#2	Energy sk#1
1	Thr0 b0	Thr0 b0	FwdLthr0 b0	Esum b0
2	Thr0 b1	Thr0 b1	FwdLthr0 b1	Esum b1
3	Thr0 b2	Thr0 b2	FwdLthr1 b0	Esum b2
4	Thr1 b0	Thr1 b0	FwdLthr1 b1	Esum b3
5	Thr1 b1	Thr1 b1	FwdLthr2 b0	Etmiss b0
6	Thr1 b2	Thr1 b2	FwdLthr2 b1	Etmiss b1
7	Thr2 b0	Thr2 b0	FwdLthr3 b0	Etmiss b2
8	Thr2 b1	Thr2 b1	FwdLthr3 b1	Etmiss b3
9	Thr2 b2	Thr2 b2	FwdRthr0 b0	Etmiss b4
10	Thr3 b0	Thr3 b0	FwdRthr0 b1	Etmiss b5
11	Thr3 b1	Thr3 b1	FwdRthr1 b0	Etmiss b6
12	Thr3 b2	Thr3 b2	FwdRthr1 b1	Etmiss b7
13	Thr4 b0	Thr4 b0	FwdRthr2 b0	*
14	Thr4 b1	Thr4 b1	FwdRthr2 b1	*
15	Thr4 b2	Thr4 b2	FwdRthr3 b0	*
16	Thr5 b0	Thr5 b0	FwdRthr3 b1	*
17	Thr5 b1	Thr5 b1	*	*
18	Thr5 b2	Thr5 b2	*	*
19	Thr6 b0	Thr6 b0	*	*
20	Thr6 b1	Thr6 b1	*	*
21	Thr6 b2	Thr6 b2	*	*
22	Thr7 b0	Thr7 b0	*	*
23	Thr7 b1	Thr7 b1	*	*
24	Thr7 b2	Thr7 b2	*	*
25	*	JetEt b0	*	*
26	*	JetEt b1	*	*
27	*	JetEt b2	*	*
28	*	JetEt b3	*	*
29	*	*	*	*
30	*	*	*	*
31	*	*	*	*
32	CLK	CLK	CLK	CLK
33	Parity	Parity	Parity	Parity
34	GND	GND	GND	GND