Preliminary Design Review of PreProcessor MCM

(ATLAS Level-1 Calorimeter Trigger)

24 January 2000

Introduction

The review was held at RAL on 24th January 2000, following the reviewers' assessment of the specification documents, which were made available on the web at:

http://wwwasic.kip.uni-heidelberg.de/~pfeiffer/ftp/PPrMCM.specX.ps

Review Panel: **Christian Bohm (Stockholm)**
Paul Bright-Thomas (Birmingham)
Viraj Perera (RAL)
Uli Schaefer (Mainz)

Also present: **Eric Eisenhandler (QMW)**
Norman Gee (RAL)
Ullrich Pfeiffer (Heidelberg)

The review started with Ullrich Pfeiffer presenting a summary of the proposed PreProcessor MCM. He described the functional role of the MCM and its location on the PreProcessor module, and showed a conceptual layout. Details of the production techniques of the proposed MCM-L (laminated) construction were then discussed and some of the important design features were emphasised, such as separation of the analogue and digital power supplies and grounds, and the factor ~2-3 reduction in power dissipation from the demonstrator MCM.

He presented a table summarising the most significant design parameters of the device, which will be constructed as a four-layer Cu-polyimide sandwich bonded to an electrically-isolated 0.8mm Cu substrate and encapsulated with a metal lid. Four of the nine dies will be FADC chips, which will require about 200 thermal vias. The complications associated with flip-chip bonding will be avoided, but almost 400 wire bonds will be needed. He explained that a functionally-correct mock-up of the device will be designed and built before submitting the final design, with the aim of optimising layout and decoupling.

He then addressed many of the issues that had been raised by the reviewers by presenting a table summarising the actions that would be taken in response by the MCM designers. The most important of these points are discussed below:

Where FADC channels are unused, their corresponding PPr ASIC LUTs will normally be set to disable them, but in order to monitor noise on these channels their inputs should be grounded as far upstream as possible.

The large substrate width (2cm) will require very close vertical packing of devices on the PPMs, with tight tolerances, but is unavoidable if the desired connectors are used. It was pointed out that there is no similar limit on the device length, although differential thermal expansion issues may impose constraints.
The exact number of devices to manufacture will depend on several factors, many of which are not yet quantified. For example, full-speed testing of the FADCs at 40 MHz would only be possible if the dies were obtainable in wafer-form, which is under discussion with the manufacturers, and overall yield would be increased if all assembly operations (die-attach, wire-bonding, surface-mount component connection, etc.) were performed by a single company. However, the proposed number appears inadequate under the guidelines of the current spares policy for customised components, so it was agreed that this spares policy should be re-examined at the forthcoming Level-1 Calorimeter Trigger Joint Meeting.
Two options for device encapsulation are still being considered - glob-top, or (preferably) a metallic lid with hermetic seal, attached with conducting epoxy, although care must be taken that this does not extend the lateral dimension of the device beyond the critical 2cm.
Single-ended clock distribution on the MCM itself is considered quite satisfactory, but at PPM board-level it should be differential with conversion close to the MCMs.
The implications of using off-MCM Virtex-E devices as alternatives to the NS LVDS serialisers have been considered, but are thought to introduce many difficulties. A third connector would be required to bring the 30 FADC output bits off each MCM, and the consequent tracking on the PPM would be extremely complex.
It was explained that the PPr ASIC would provide the necessary SYNC1/2 and PWRDWN signals for the three LVDS Tx chips, so no signals external to the MCM would be needed.
Further details of the electrical connections to the dies were described. Flip-chip techniques will not feature at all, and wire-bonding will be used universally, with 25 micron Al wires.

Recommendations

The reviewers then discussed some of the issues that they felt needed further clarification, and presented their conclusions to Ullrich Pfeiffer. In summary, the recommendations of the review panel are as follows:

1. The MCM analogue input signals are attenuated by an RC network which relies on the input impedance of the FADC devices. As this has a tolerance of up to +/-20% it would introduce an error of +/-10% in the calibration, which is unacceptable.

- An alternative attenuation network should be designed, with a target tolerance of +/-1%.

2. The panel learnt that the PHOS4 programmable delay ASIC, used on the MCM to produce correctly-timed strobes for the four FADCs, has exhibited a serious problem on test. If it experiences a momentary loss of input clock it appears to lose all its programmed timing settings, which go to full-delay, although the four delayed clocks are still present. There are two serious consequences:

a) loss of timing calibration settings, with no warning to the user
b) inability to reset the device except via a very intrusive power down-up sequence

- Further information should be obtained on the conditions under which this effect occurs.
- Techniques to monitor the occurrence should be investigated.
- Alternative procedures to reset the device should be considered.
- The implications for the MCM design of re-designing the device should be considered.

3. The NS LVDS serialiser requires a clock jitter <150 psec, whereas the current TTCrx Reference Manual and some recent lab measurements both indicate a peak-to-peak de-skewed clock jitter of up to 250 psec. This could prove a potentially serious source of link errors.

- Investigate the use of an additional low-jitter PLL, to be used at PPM board-level.
- Extend the recent LVDS link tests (Birmingham, Heidelberg, Mainz) to use the TTC system as a clock source.
- Investigate the possible use of the recently-announced faster NS LVDS serialiser chipset.

4. Knowledge of the detailed sequence of MCM manufacturing and assembly steps is important to ensure that successive processes are compatible.

- Include greater detail about the full manufacturing sequence (and subsequent testing).

5. The choice of the most suitable FADC chip is very important.

- Include a justification of FADC choice (or add a reference to previous studies of FADC devices).

6. The 480 Mbaud bitstream outputs from the LVDS serialiser dies must be transported with great care to avoid reflections and consequent increased bit-error rates.

- The MCM specifications should define the LVDS output traces to be 100 ohms differential impedance.

7. Experience from the recent LVDS link tests (Birmingham, Heidelberg, Mainz) indicates that the LVDS serialiser environment is crucial for optimum performance (low bit-error rates, etc.).

- Specify the power supply decoupling requirements in more detail.

8. Low bit-error rate operation of the LVDS links over long cables depends crucially on the use of appropriate cable drivers coupled with pre-compensation networks, all at PPM board-level. The precise nature of these components may influence the design of the LVDS-related section of the MCM.

- The off-MCM LVDS fan-out and cable pre-compensation scheme should be thoroughly understood and demonstrated before the MCM design is frozen.

9. MCM assembly requires working PPr ASICs and the completed devices are also the most important components of the PPMs, carrying the majority of their functionality. Therefore the design and manufacture of the PPr ASIC, the MCM and the PPM are all heavily inter-dependent.

- A work-plan schedule for the MCM design and manufacture should be provided, clearly showing the relevant time-links into the PPr ASIC and PPM schedules.

10. If serious problem to the use of the NS LVDS serialiser chipset were to be found, the only demonstrated alternative link technology would be H-P G-link.

- Consider the implications for the MCM design of reverting to G-link dies.

A.R.Gillman   11-02-2000