16th September 1998

ATLAS Level-1 Calorimeter Trigger

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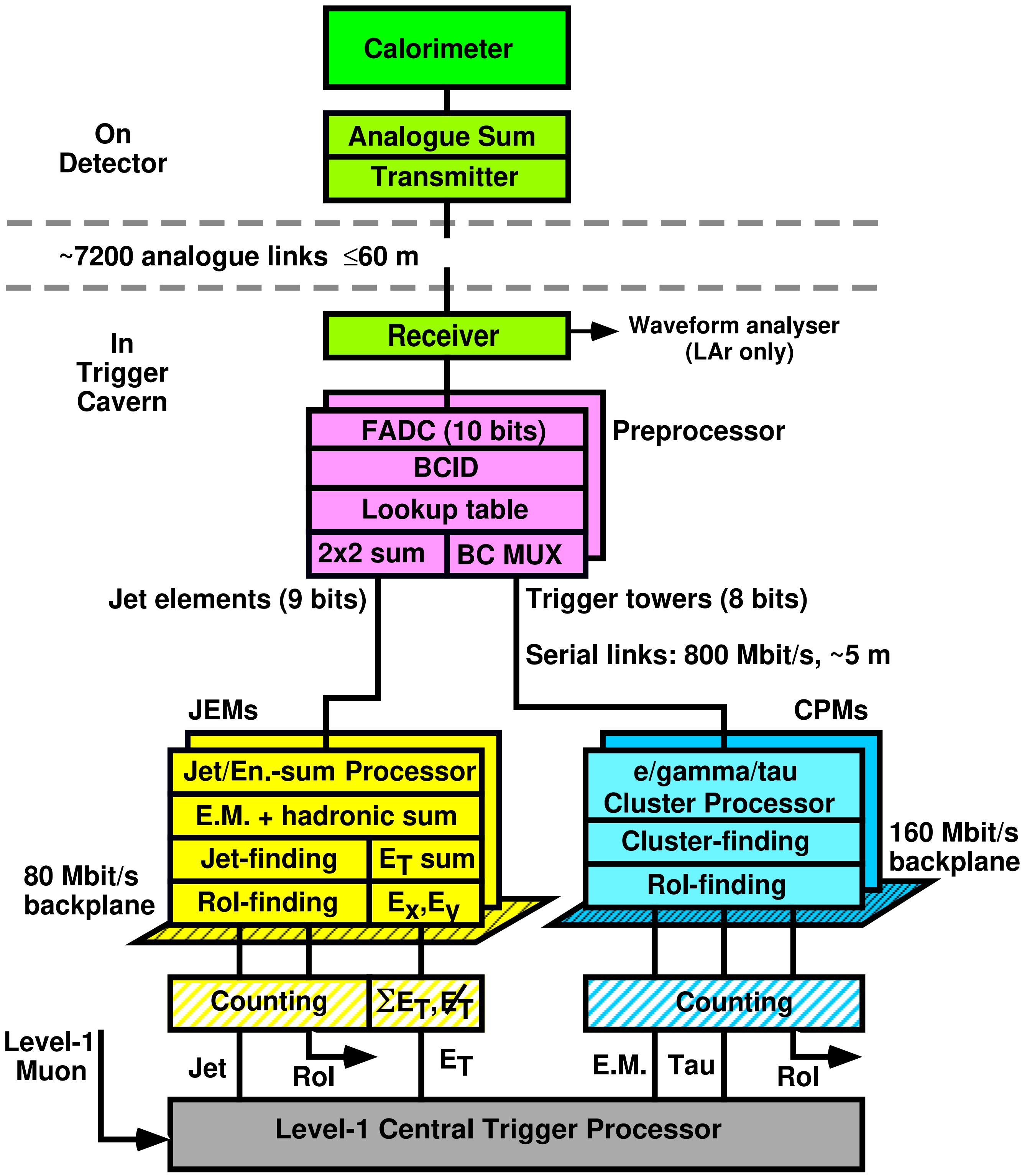
Trigger Architecture



Calorimeter input signals

- **Trigger towers are sums of calorimeter cells, both laterally and in depth. Up to 60 cells (LAr e.m. barrel) must be summed to make up each tower.**
- **Towers are 0.1 $\times$ 0.1 in $\eta \times \phi$ for $|\eta| < 2.5$ and typically 0.2 $\times$ 0.2 for $|\eta| > 2.5$.**

Trigger type	Granularity	η coverage	Trigger elements
electron/photon hadron/tau	~ 0.1 $\times$ 0.1	$\|\eta\| \leq 2.5$	~6400
Jet	~ 0.2 $\times$ 0.2	$\|\eta\| \leq 3.2$	~1920
missing-E_T sum-E_T	~ 0.2 $\times$ 0.2	$\|\eta\| \leq 4.9$	~1986

- **Digitization is 10 bits, 40 MHz, ~0.25 GeV E_T per count.**
- **Lookup table corrects E_T calibration, subtracts pedestal, applies a noise threshold.**

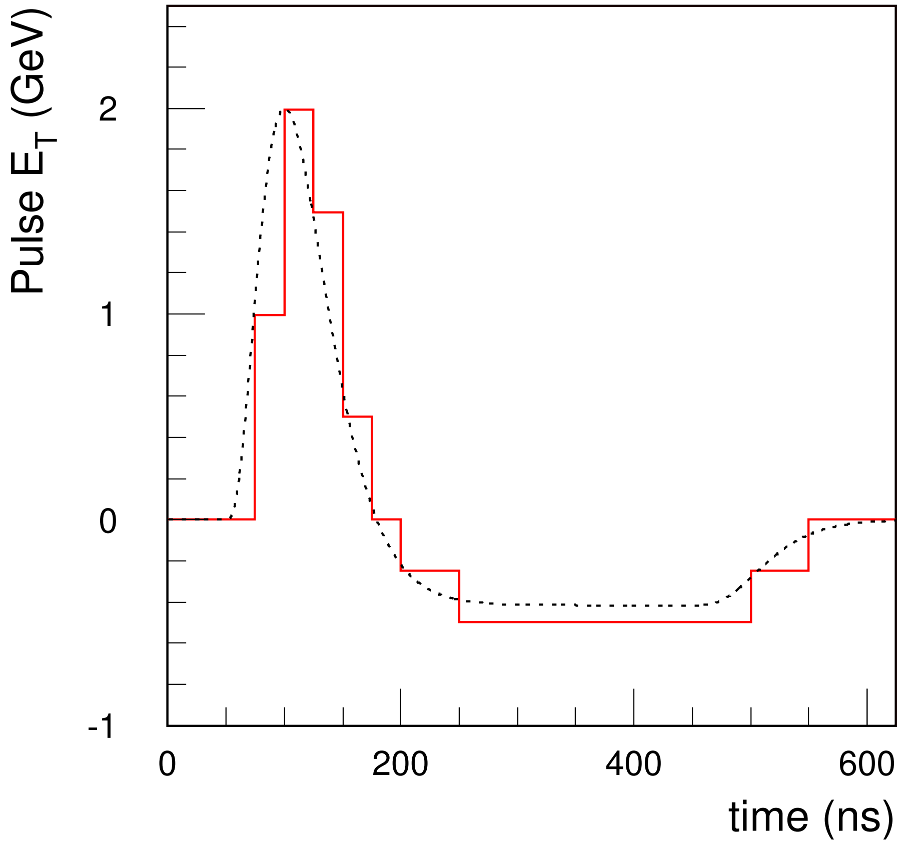
- **Cluster Processor inputs:**
  8-bit data, 0.1 $\times$ 0.1, ~1 GeV E_T per count.
- **Jet/Energy-sum Processor inputs:**
  9-bit data, separate 0.2 $\times$ 0.2 e.m. and hadronic sums, ~1 GeV E_T per count.

Bunch-crossing identification (BCID)

Wide calorimeter pulses require that we accurately:

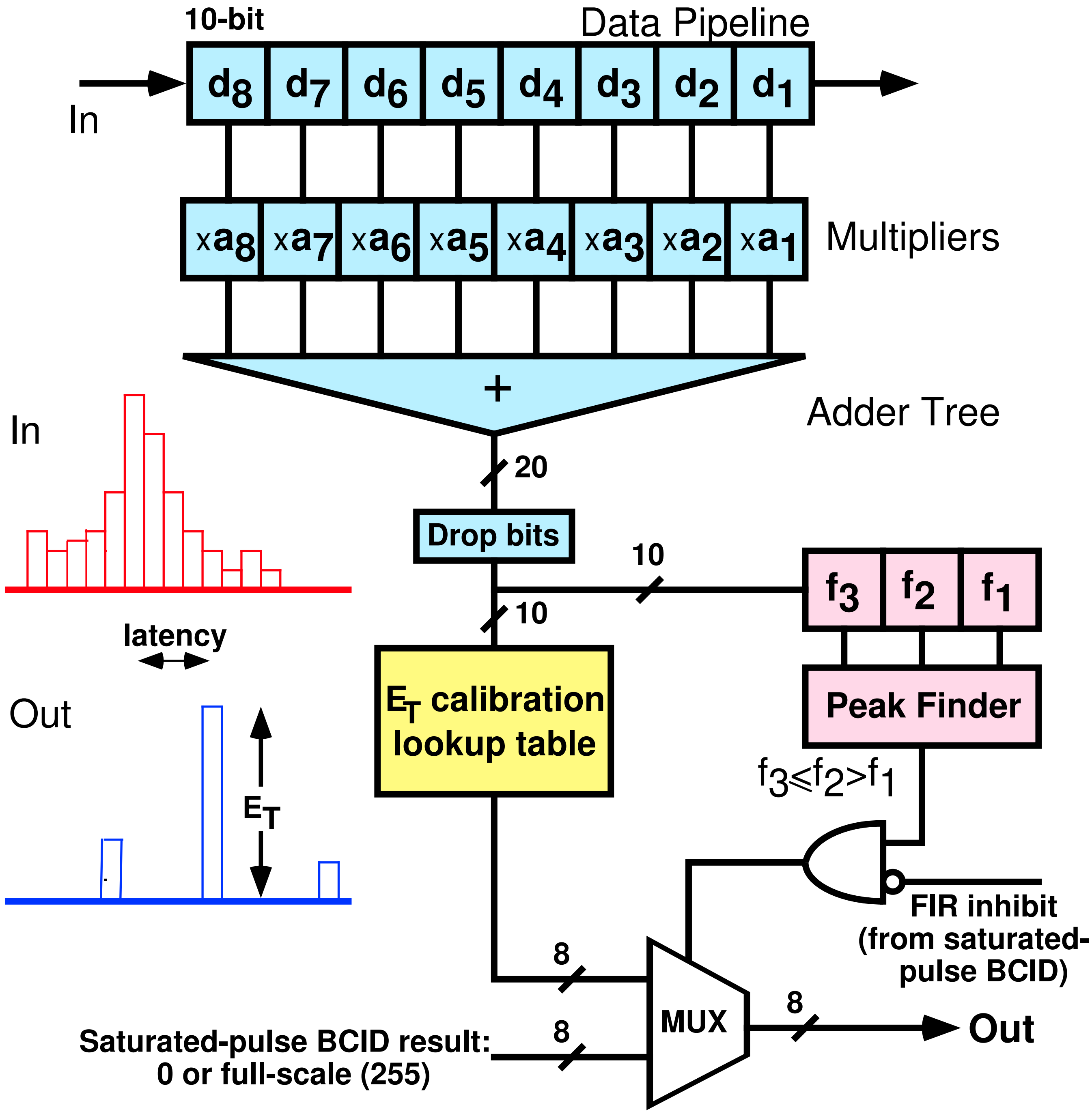
- **identify bunch-crossing for each trigger tower with significant energy deposition**
- **extract correct transverse energy**

This drives many of the requirements on calorimeter input signals, such as constant pulse shape.



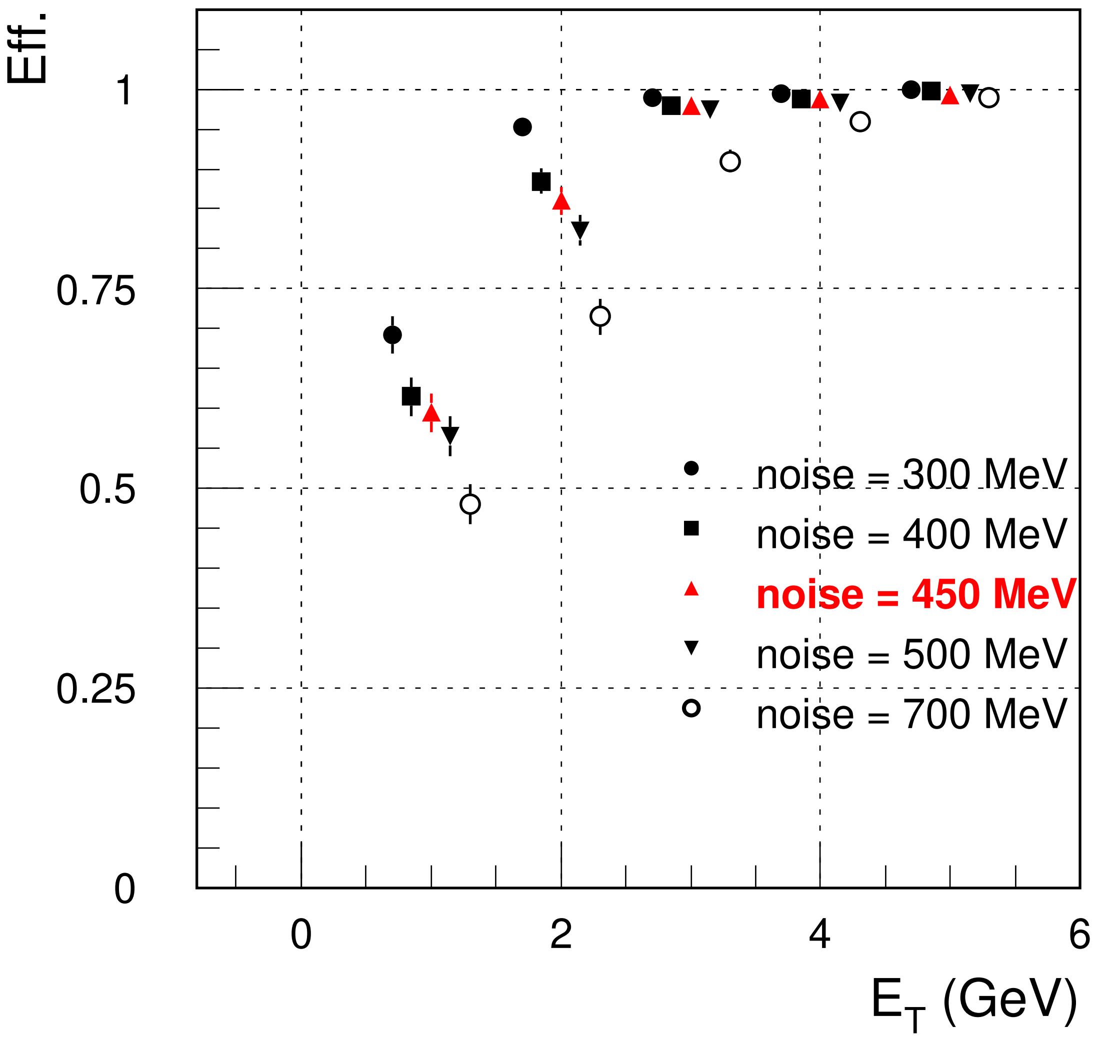
BCID (continued)

Method for unsaturated signals is pipelined finite impulse response (FIR) filter followed by a peak-finder:



BCID (continued)

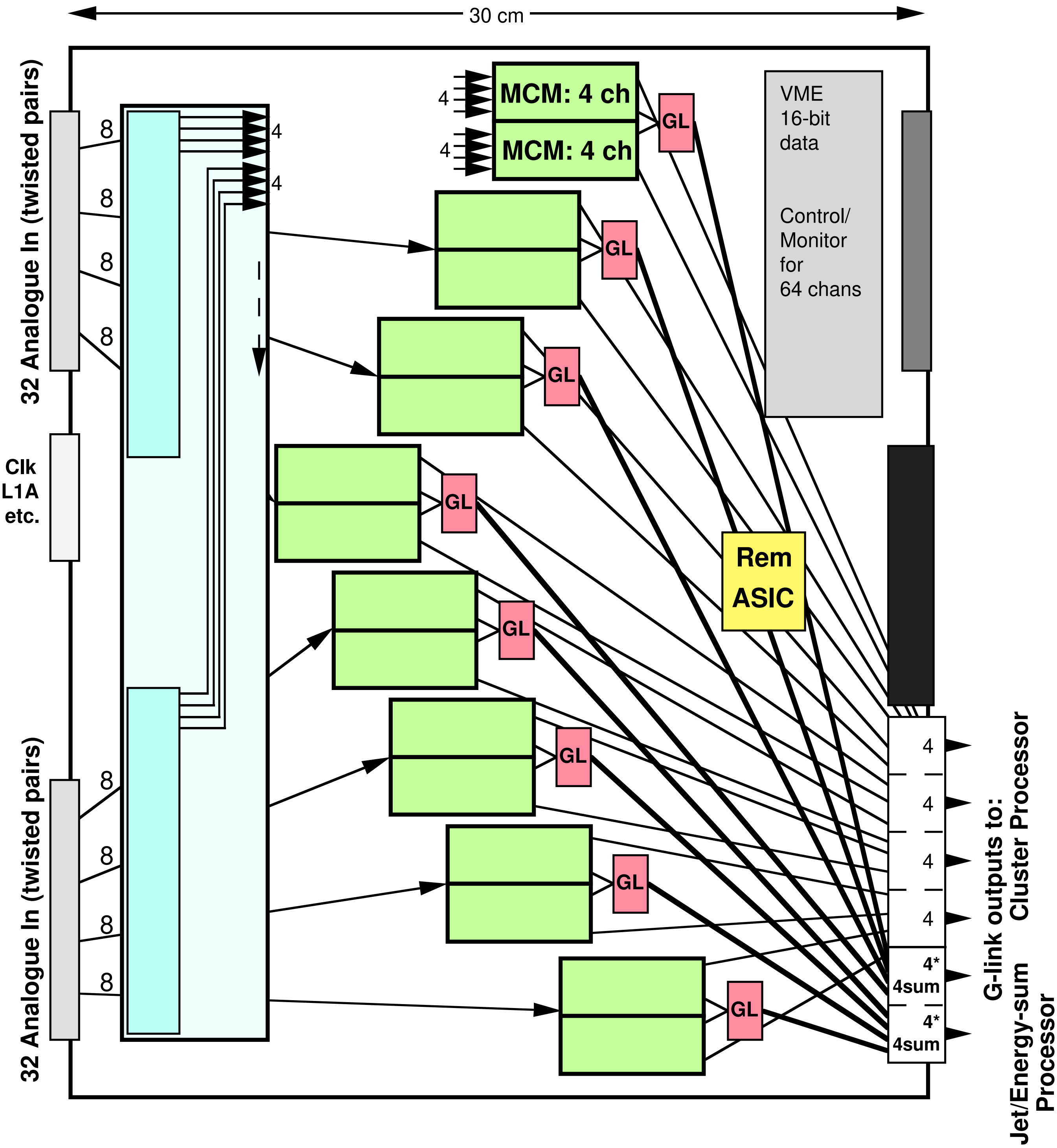
Example of BCID performance simulation. Method is efficient down to E_T ~ 2 GeV.



Note: points displaced for visibility.

Preprocessor

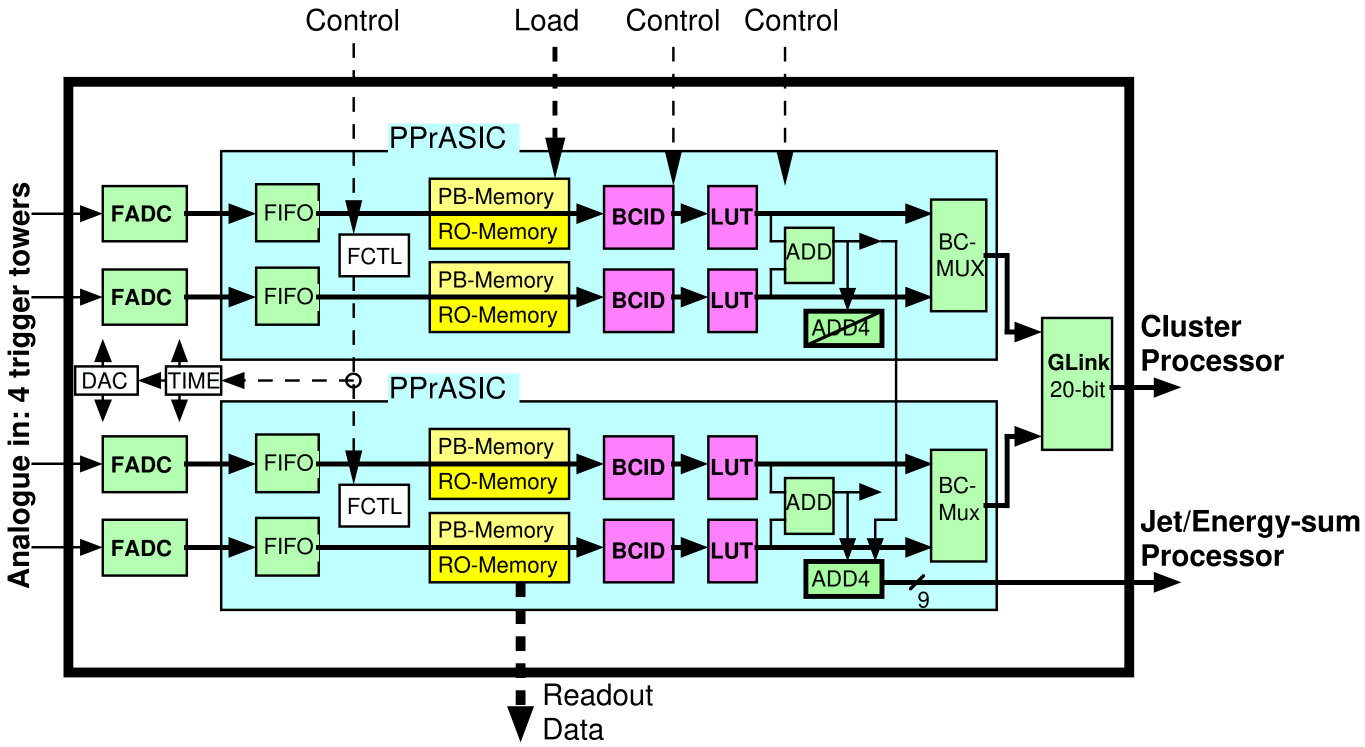
Preprocessor module:



- 64 trigger towers per 9U module.
- 8 crates of 16 modules needed.

Preprocessor (continued)

Preprocessor multi-chip module:

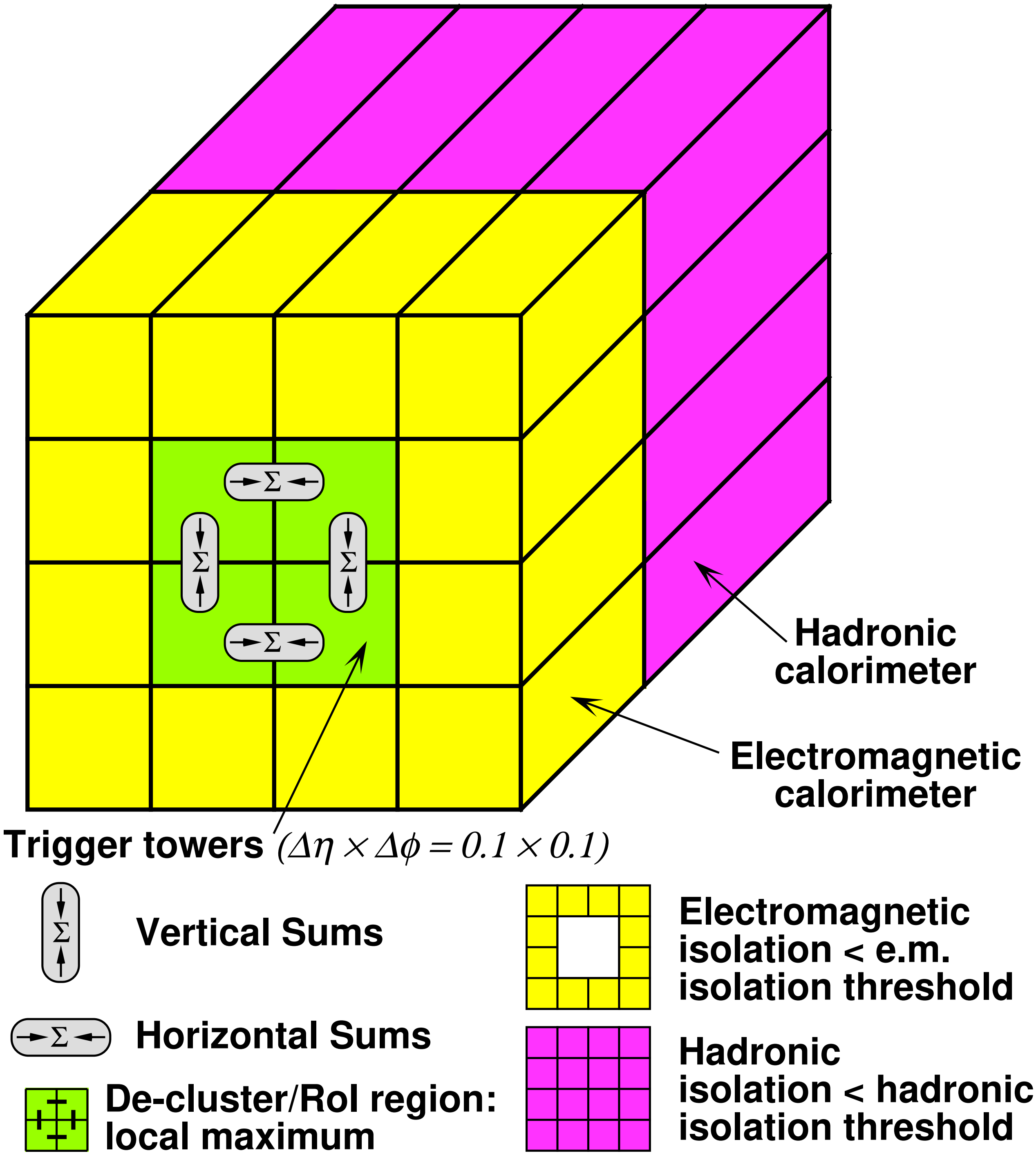


Functions:

- **Digitize signals with accurately-timed strobe.**
- **Synchronize to same bunch-crossing.**
- **Store values for readout over several bunch-crossings (also allows input for test/playback).**
- **Perform bunch-crossing identification.**
- **Calibration lookup table: subtract pedestal, calibrate E_T, apply noise threshold. (Output stored for readout.)**
- **Transmit in serial format to Cluster Processor with G-link.**
- **Pre-sum 0.2×0.2 regions for serial transmission to Jet/Energy-sum Processor.**

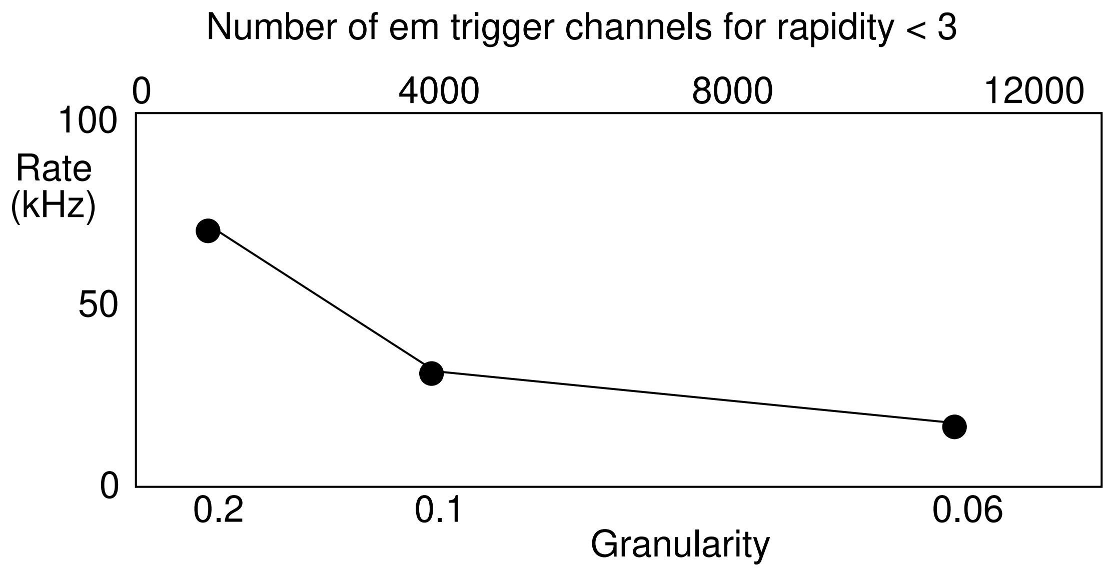
Electron/photon trigger algorithm

- Most challenging part of trigger — must reject the overwhelming QCD jet background.



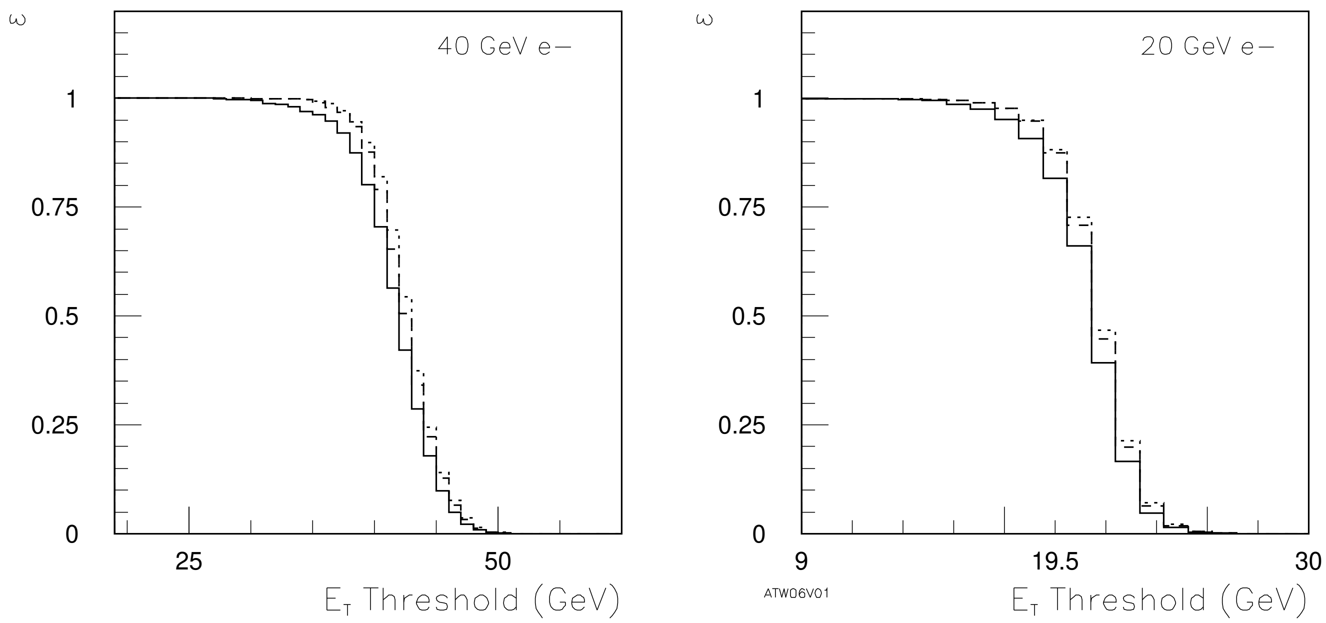
- ≥1 vertical or horizontal sum > cluster threshold E_T.
- E.M. and hadronic isolation conditions satisfied.
- Central 0.2 x 0.2 region must be E_T local maximum compared to its 8 overlapping neighbours. This does de-clustering and defines RoIs.

Trigger Cell Size



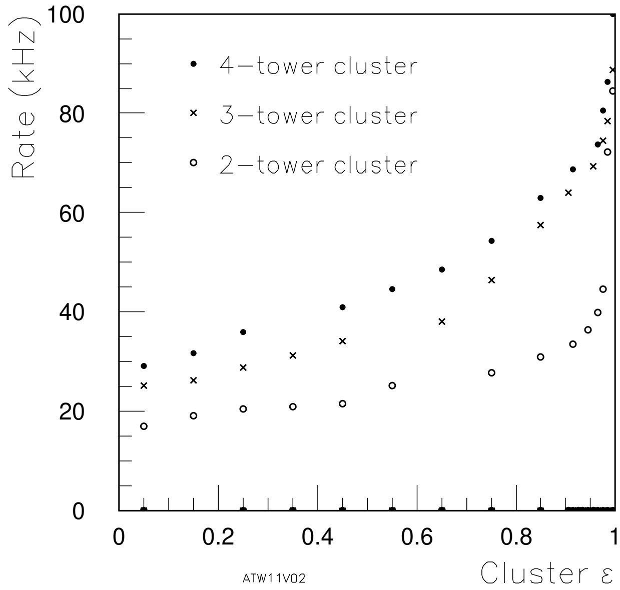
Inclusive electron/photon trigger rate vs tower granularity, for a threshold of 40 GeV and LHC design luminosity, using a 2-tower cluster without isolation.

Electron Cluster Definition



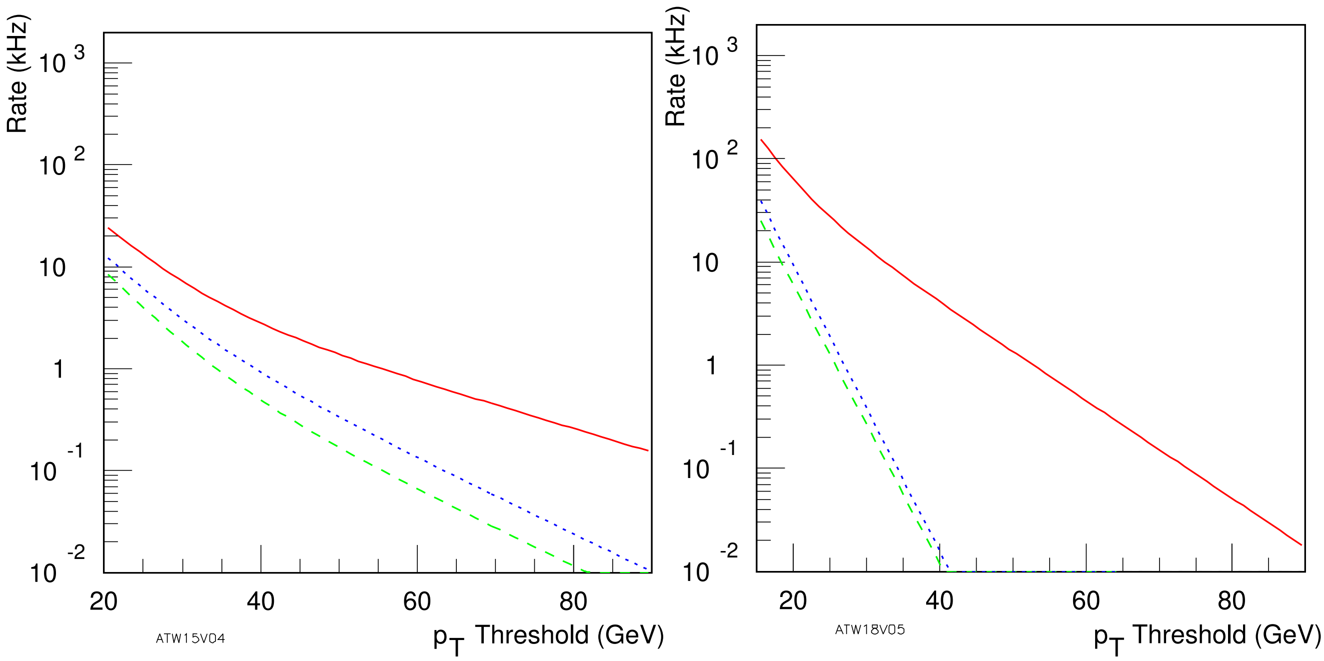
Cluster efficiency curves for three different cluster definitions for 40 and 20 GeV electrons. Solid = 2 towers, dashed = 3, dotted = 4..

Electron rates



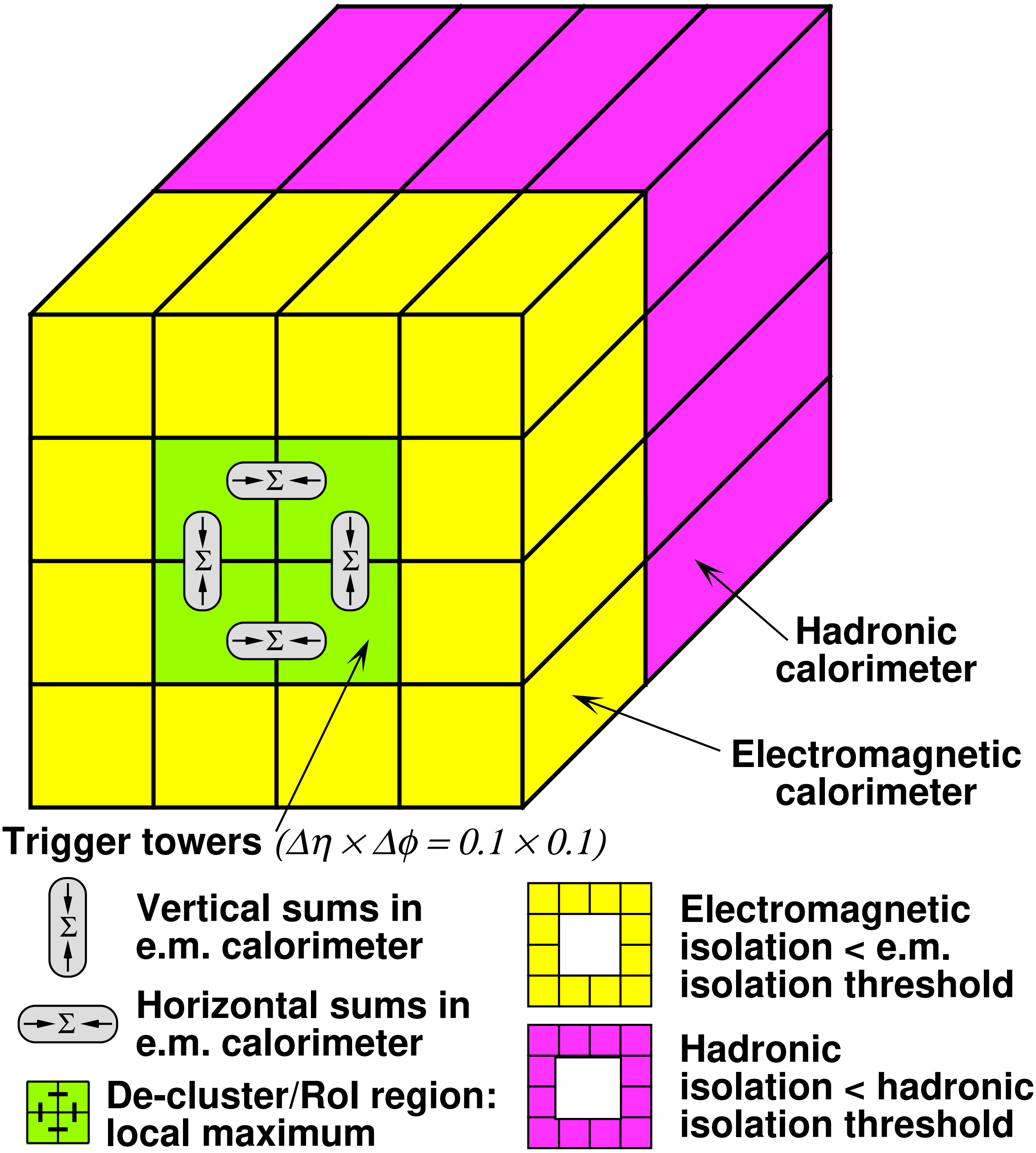
QCD background rate vs efficiency for 40 GeV electrons, at design luminosity

Electron Isolation



Electron/photon trigger rates, with no isolation (solid), hadronic isolation only(dotted), and full isolation(dashed). Inclusive rates (left) at 10% luminosity, electron pairs (Right) at full LHC design luminosity

Hadron (τ) trigger algorithm

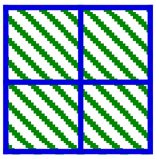


- $\geq$1 vertical or horizontal sum > cluster threshold E_T.
  (hadronic sum might be 2×2 not 2×1)
- E.M. and hadronic isolation conditions satisfied.
- Central 0.2 x 0.2 region must be E_T local maximum compared to its 8 overlapping neighbours.
  This does de-clustering and defines RoIs.

Jet algorithms

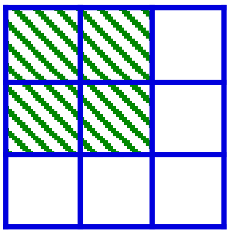
Separate Programmable Choice per Threshold

Window 0.4 x 0.4
Jet element/Slide 0.2 x 0.2
De-cluster/RoI 0.4 x 0.4, overlapping



> Jet Threshold

Window 0.6 x 0.6
Jet element/Slide 0.2 x 0.2
De-cluster/RoI 0.4 x 0.4, overlapping

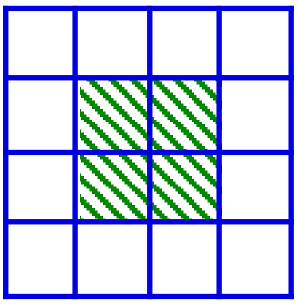


> Jet Threshold

De-cluster/RoI can be in 4 possible positions

Note: De-cluster/RoI region is defined to be a local maximum in E_T

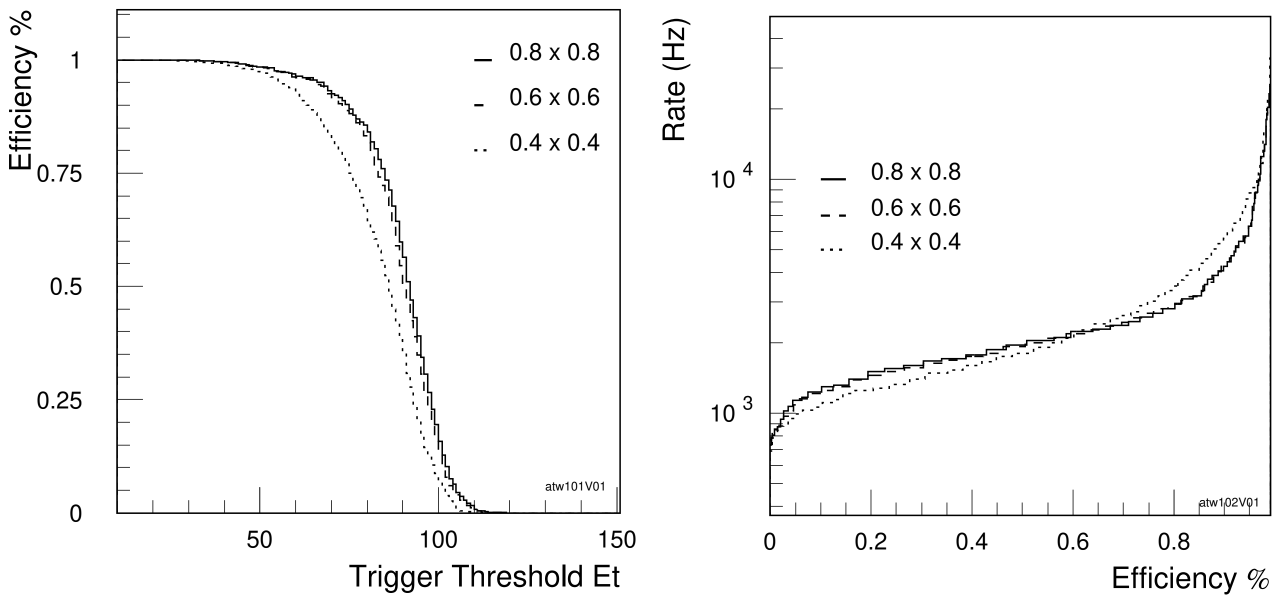
Window 0.8 x 0.8
Jet element/Slide 0.2 x 0.2
De-cluster/RoI 0.4 x 0.4, overlapping



> Jet Threshold

De-cluster/RoI must be in centre position (to avoid 6x6, and 2 jets/window)

Jet Threshold and Efficiency



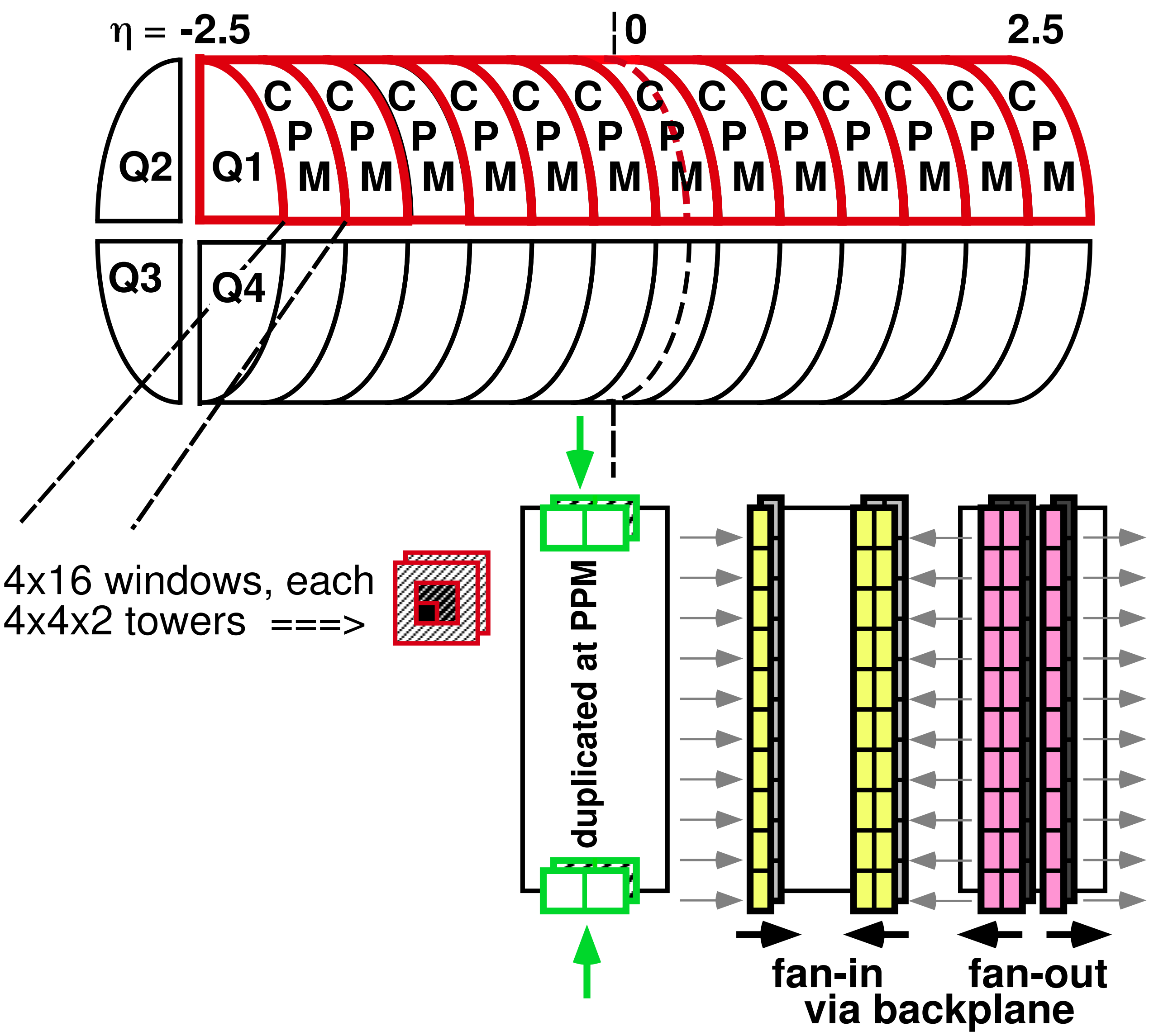
Jet trigger efficiency curves for 100 GeV ET Jets, and rate vs efficiency at 10 percent design luminosity, for three different jet cluster sizes.

Fanout

- Electron/photon, hadron/tau and jet triggers all use sliding, overlapping windows.
- Each trigger element participates in 16 different windows.
- This implies massive fanout of digital signals, and this drives the design of the trigger hardware.
- Pin counts on both chips and modules are kept feasible by extensive use of serialization.
- Careful partitioning is necessary in order to keep interconnections as simple as possible.

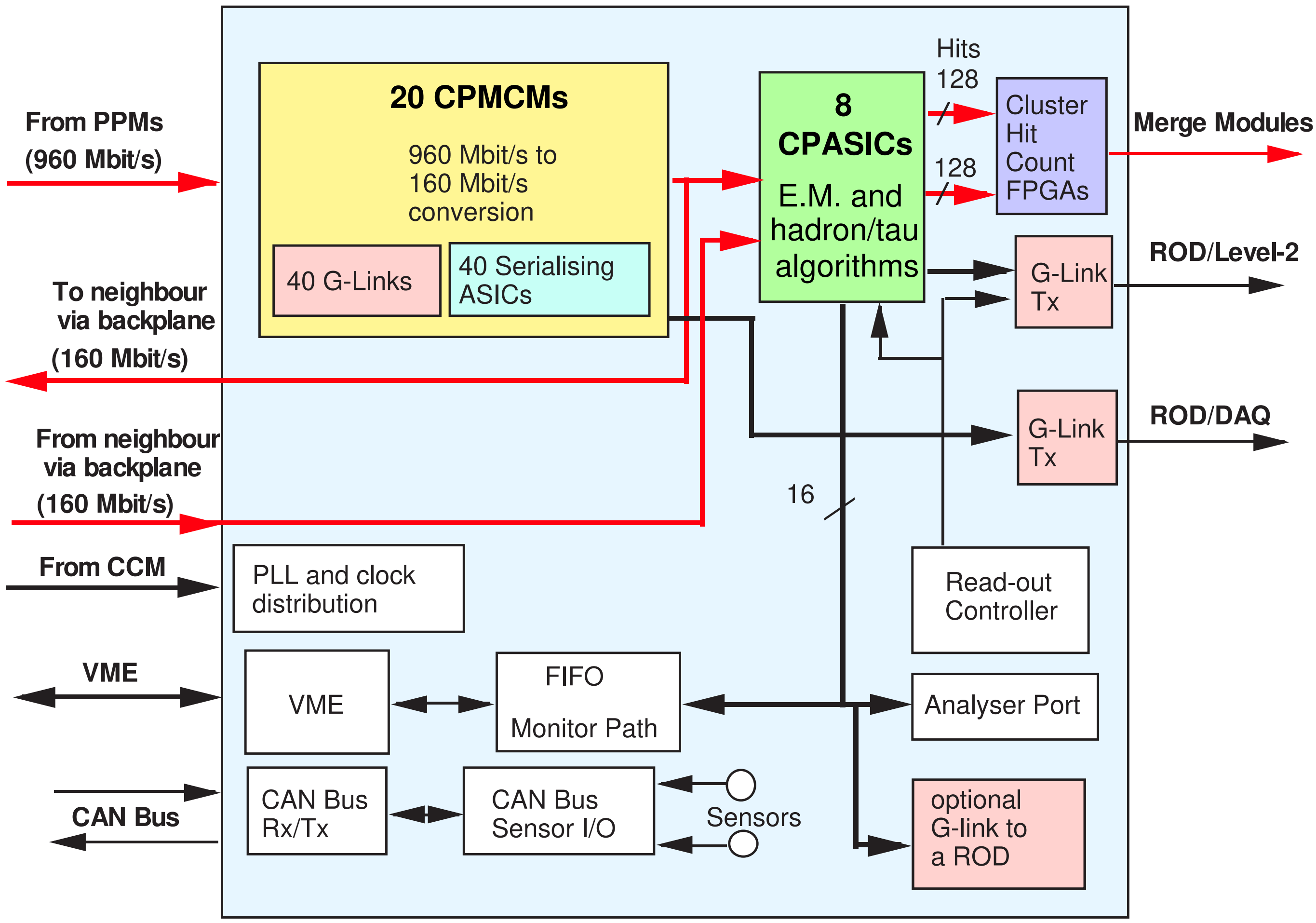
Cluster Processor (e.m. & hadron/τ triggers)

- The basic layout of the processor is quadrants in ϕ, with one crate per quadrant. Modules each cover 90° in ϕ.
- Trigger-tower inputs are serial, using e.g. H-P G-links. Use of empty bunch-crossings ('BC-MUX') reduces number of G-links (pin-count, power, cost, ...) to ~40/module.
- Module-to-module fanout is done on a backplane, using two serial lines/trigger tower at 160 Mbit/s single-ended. ϕ-quadrant layout allows 1D backplane; each CPM only communicates with 2 nearest neighbours. (Was 2D in TP)



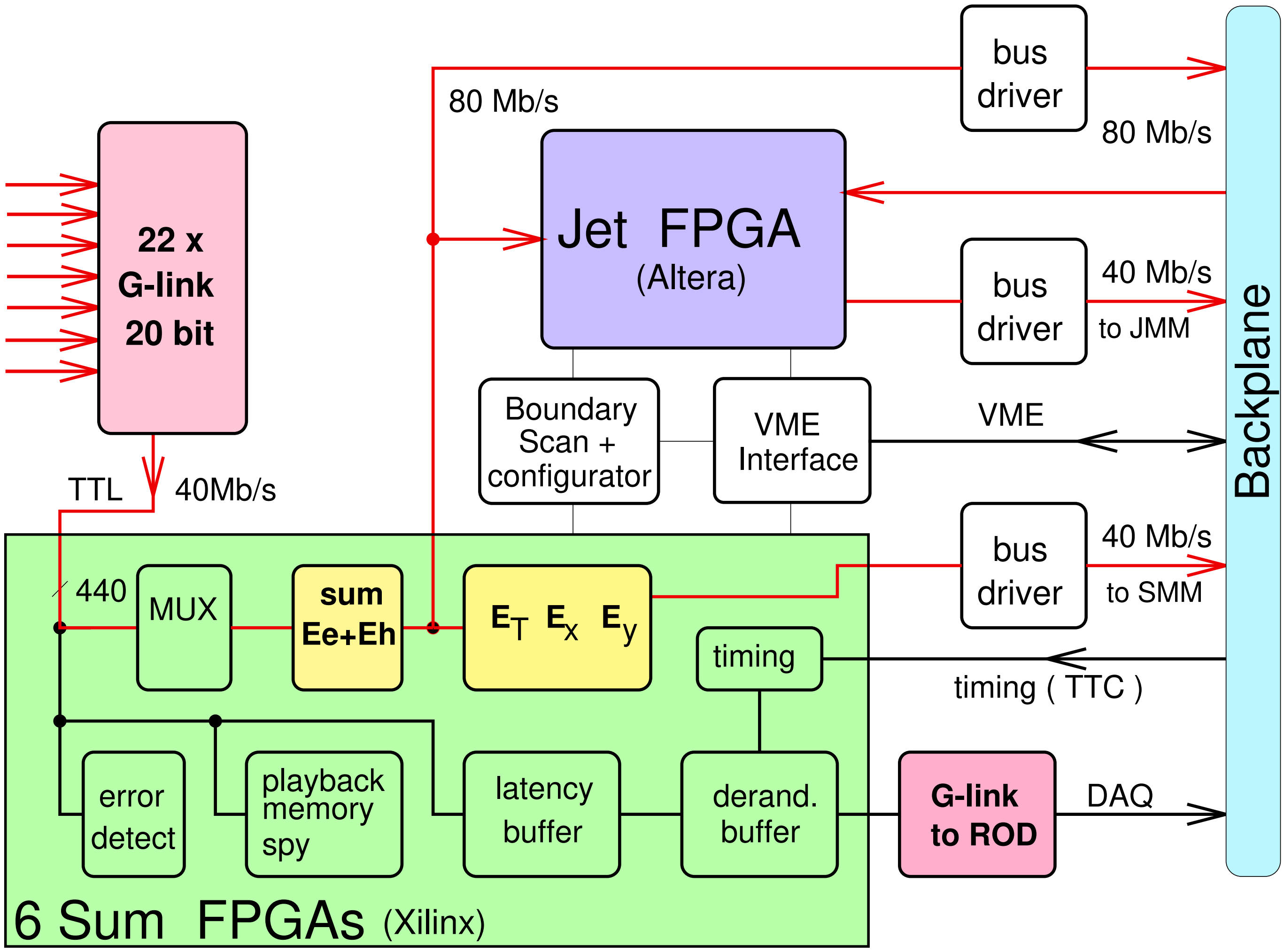
Cluster Processor Module

- **Very compact due to use of MCMs and ASICs**
- **CPASIC handles 2 $\times$ 4 windows**



Jet / Energy-sum Processor

- **Input elements are serial, using H-P G-links.**
- **They are 0.2 × 0.2, e.m. and hadronic separate, 9 bits.**
- **Cannot use bunch-crossing MUX since elements are sums of signals.**
- **Jet-finding is done on FPGAs.**
- **FPGAs and backplane run at 80 MHz.**
- **The basic layout of the processor is quadrants in ϕ:**
  - **Missing-E_T calculations in each crate can be unsigned**
  - **Backplane is 1D and only connects nearest neighbours**
- **Jet/Energy-sum Module:**



CTP output bits

- **Electron/photon: 8 threshold combinations $\times$ 3-bit multiplicity**
- **Single-hadron/tau: 8 threshold combinations $\times$ 3-bit multiplicity**
- **Jet: 8 threshold combinations $\times$ 3-bit multiplicity**
- **Missing-E_T: 8 threshold status bits**
- **Total-E_T: 4 threshold status bits**

Research & development

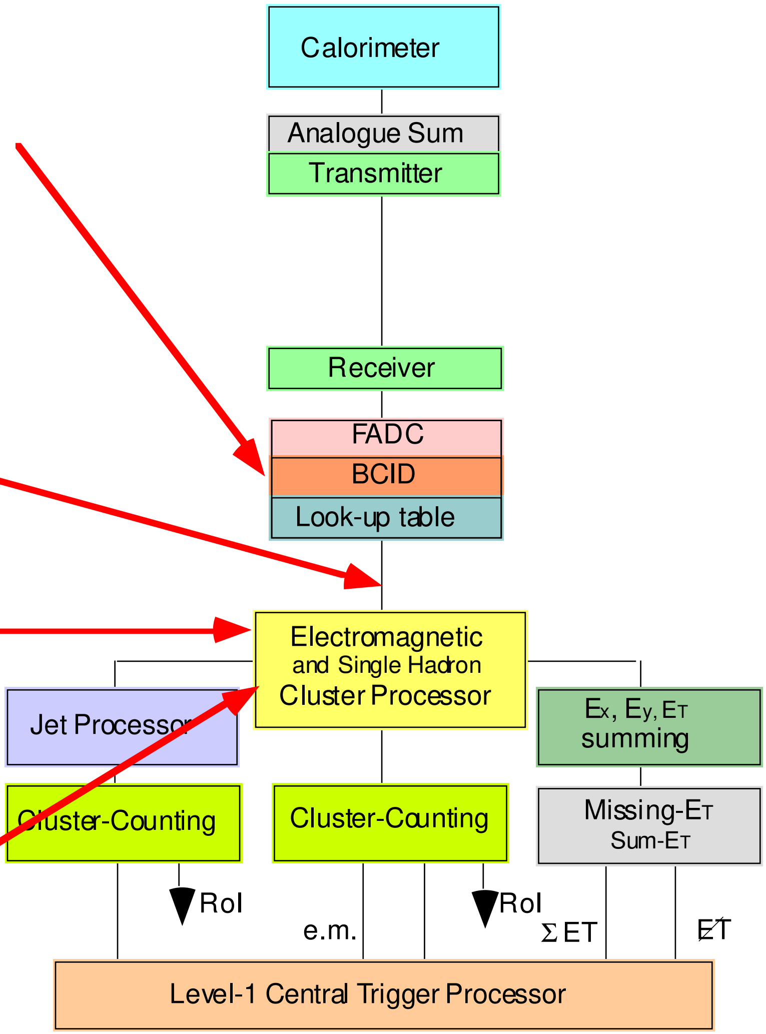
- **Beam Tests have been carried out in 1993, 1994, 1995, 1996 and October 1997, with both LAr and TileCal. Some highlights...**

1995
Efficient bunch-crossing identification (BCID) at 40 MHz

1996
Electrical (& optical) links run at 800 & tested at 1600 Mbaud

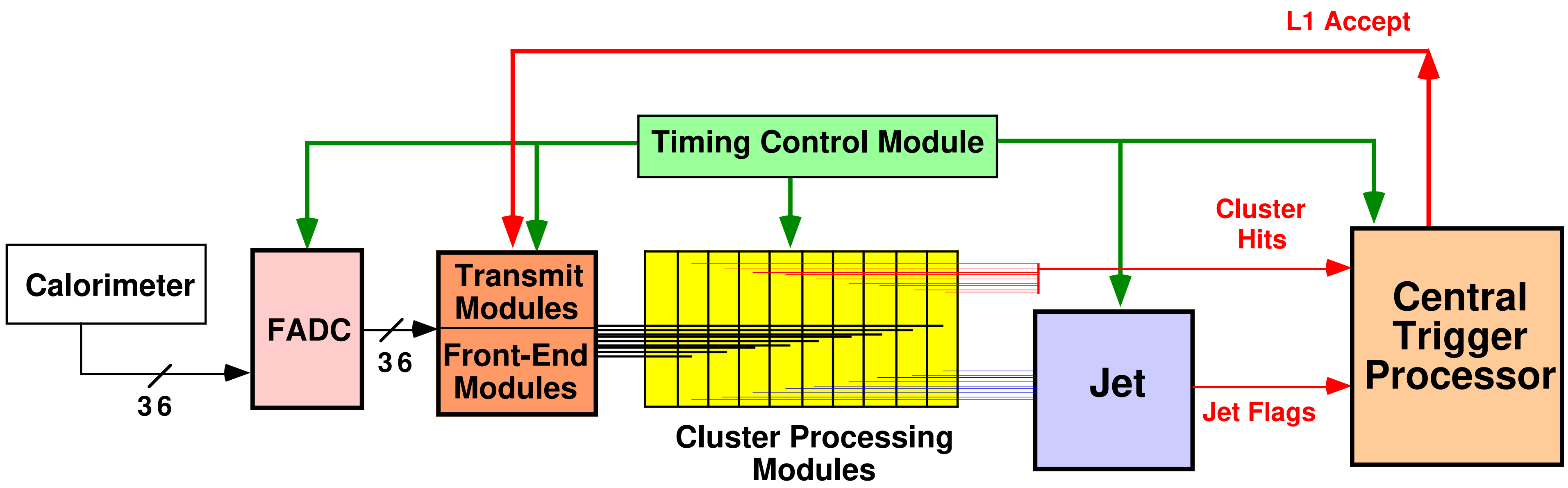
1994
E.M. cluster-finding in pipelined 40 MHz ASIC

1996
Multiplexing ASIC sending & receiving data at 160 Mbit/s



1998
System Link & Backplane Error rates measured.
BER < 10^{-12}

Complete Slice Test 1997



Level-1 Calorimeter Trigger conclusions

- **Algorithms for the trigger have been chosen and optimized using detailed simulation of detectors and trigger logic**
- **The TDR documents a Complete & Detailed system design**
- **Lengthy demonstrator work over the last 5 years underpins the architecture**
- **All the required technology exists and responsible groups have the required experience**
- **Speed and Performance meet the ATLAS physics and detector requirements**