ATLAS LVL1 Calorimeter Trigger Cluster Processor

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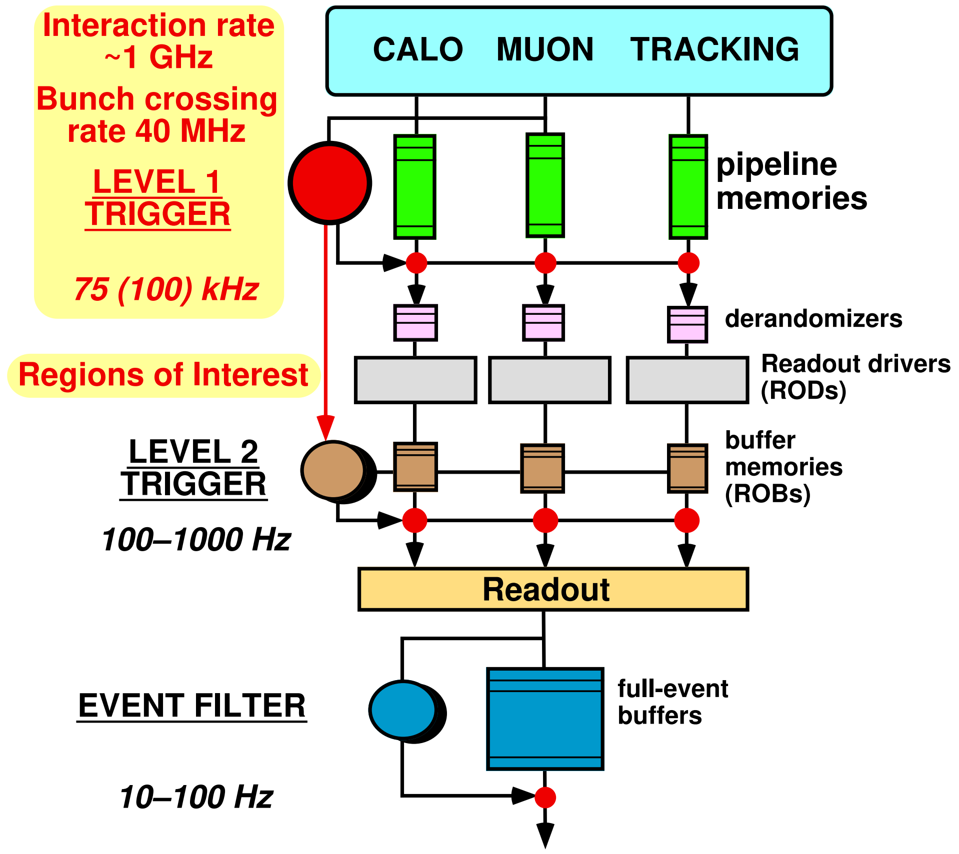
- Introduction
- CP Algorithms
- 1997 Demonstrator Programme
- CP Architecture
- Summary and Conclusions

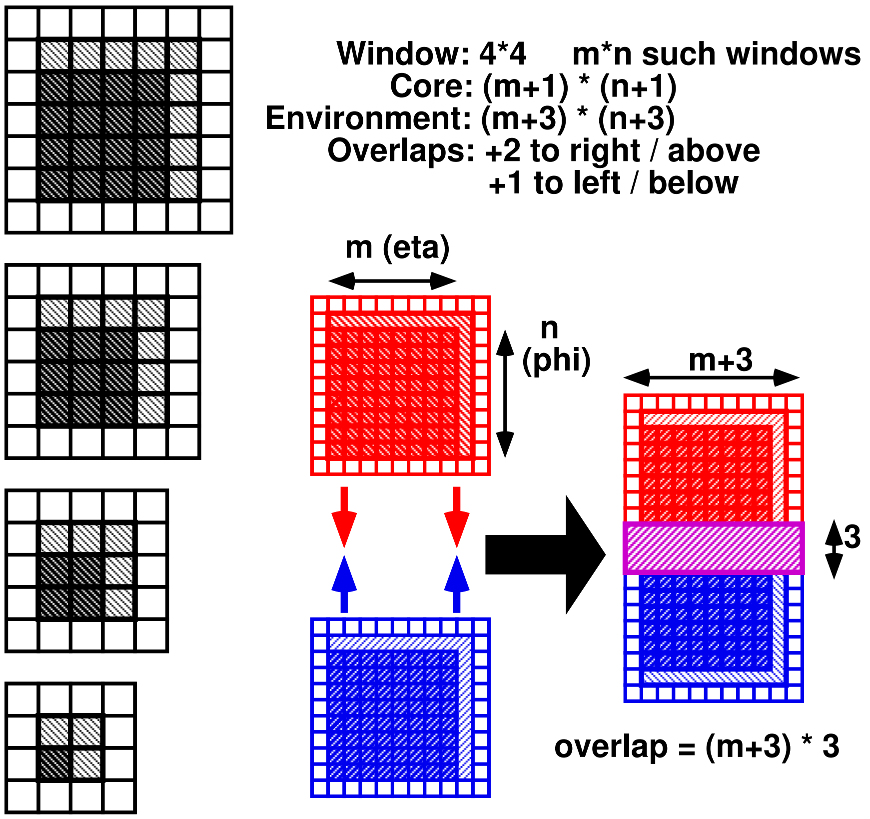
Introduction

- LVL1 Calorimeter Trigger is crucial part of ATLAS
- Must select all physics signatures other than $\mu^{\pm}$:
  - Isolated electrons and photons
  - Isolated hadrons from τ decay
  - Jets
  - $\not{E}_T$ and $\sum E_T$
- Total LVL1 factor-500+ rejection of background
- Total LVL1 latency $<$2 μs incl. $\sim$150 m cables



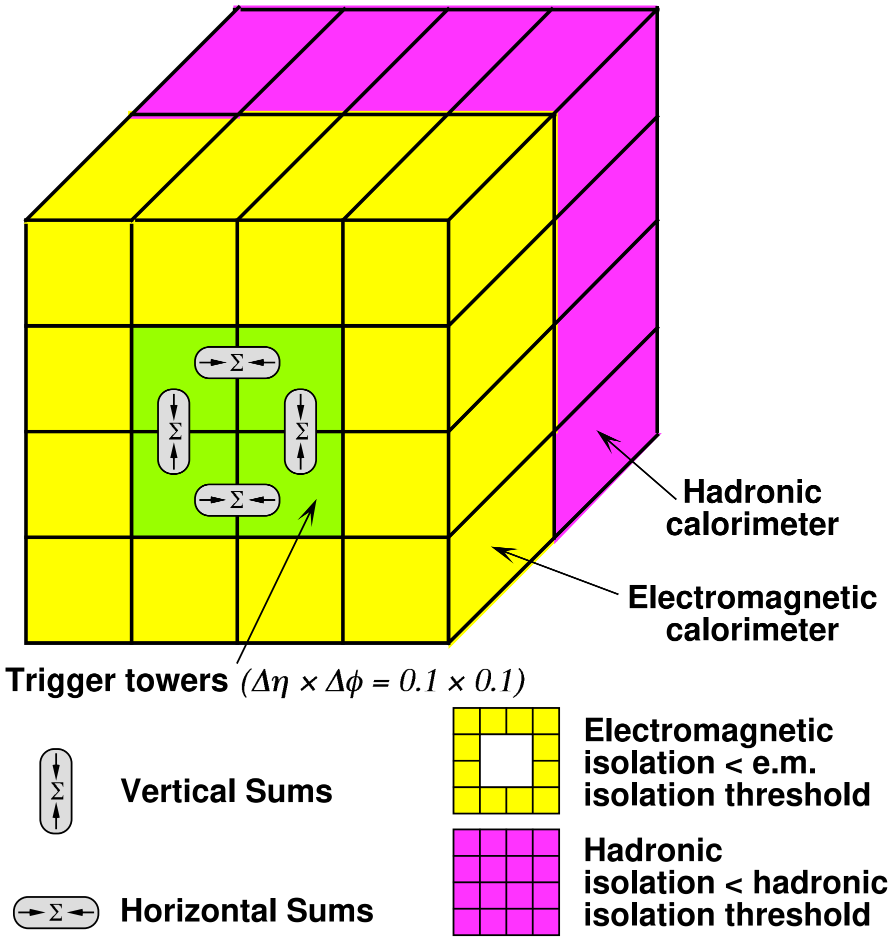
CP Algorithms

- Calorimeter signals summed to “towers” on scale of em shower
- Isolate energy deposits within local environment
- 4*4 window simplest to provide:
  - uniform efficiency across a tower
  - $\eta - \phi$ isotropy
  - 360° isolation around a cluster
- Trigger space covered by sliding window algorithm $\Rightarrow$fan-out of each signal to multiple windows
- Fan-out best performed “downstream”
- Partitioned into subspaces, non-zero overlaps



e/γ algorithm

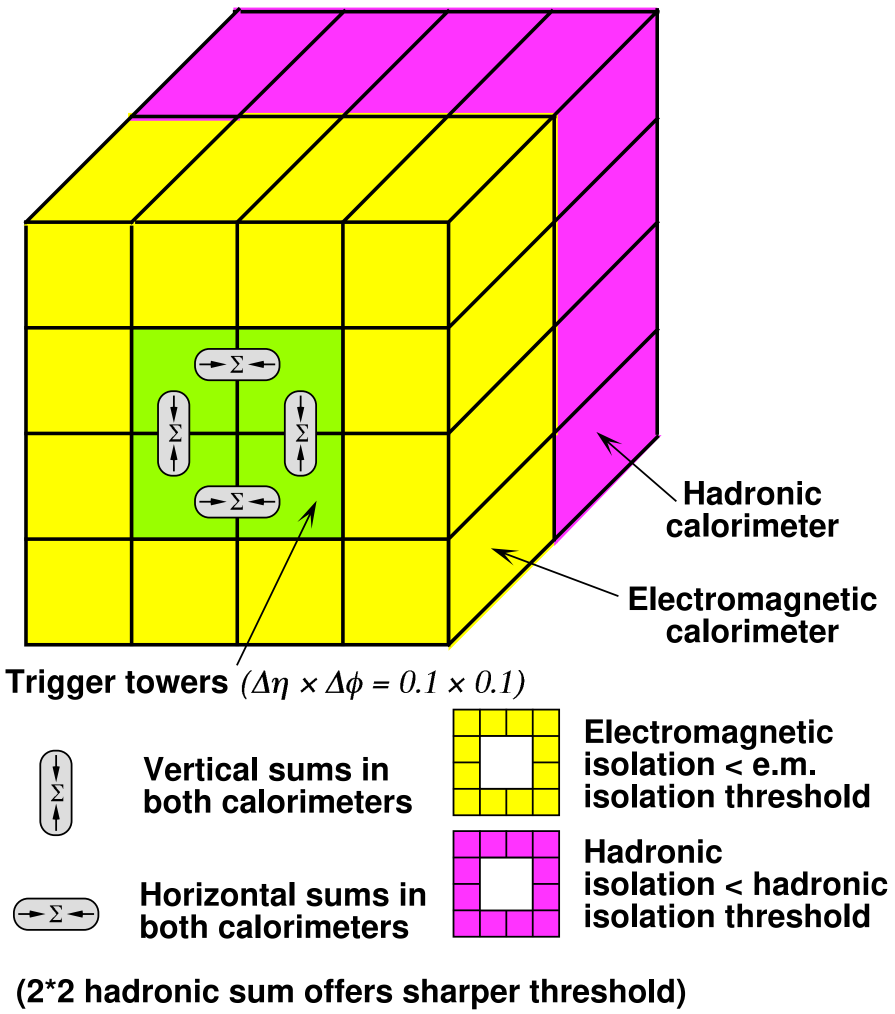
- Rejection of jet background down to low E_T



- Efficiency and rate uniform across tower and up to acceptance edges
- Each cluster discriminated at 8 threshold sets: $\left\{T^{em}_{clus,i}, T^{em}_{iso,i}, T^{had}_{iso,i}\right\}$
- Background rate studies in progress

Isolated hadron (τ) algorithm

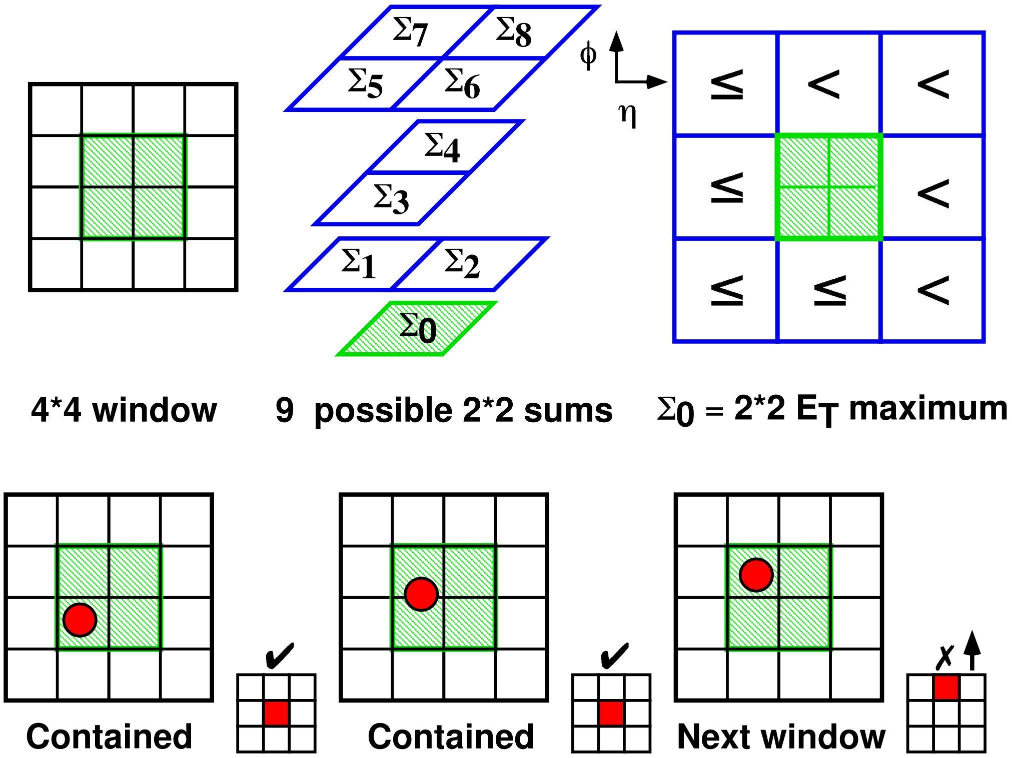
- Similar algorithm for isolated hadrons



- Larger hadronic cluster offers sharper threshold
- Separate isolations offer better discrimination and flexibility
- Small addition to CP ASIC functionality/output
- Each cluster discriminated at 4 threshold sets: $\left\{T^{em+had}_{clus,i}, T^{em}_{iso,i}, T^{had}_{iso,i}\right\}$
- Efficient for 1-prong and 3-prong τ-decays

New Decluster/RoI Algorithm

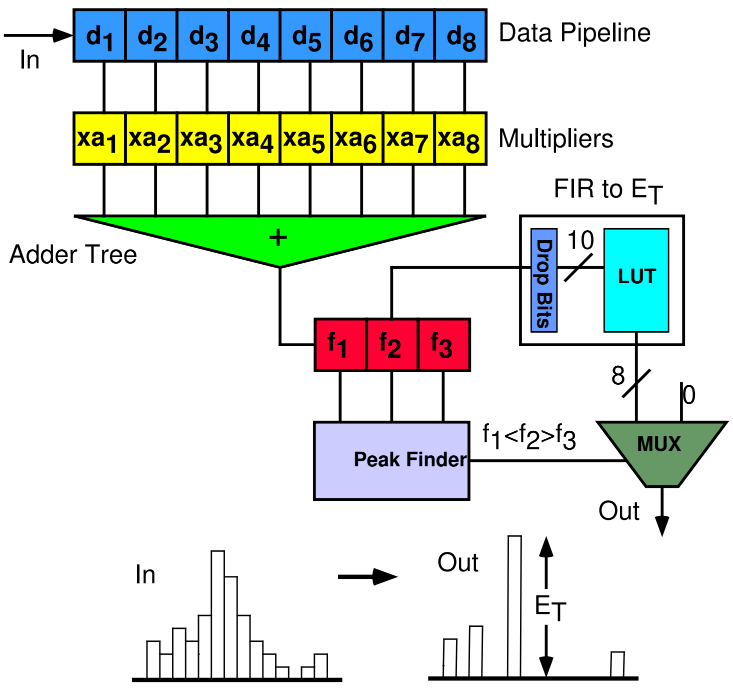
- New decluster/RoI algorithm: any cluster must be 2*2 local E_T maximum within 4*4 window



  - automatic elimination of double-counting
  - inter-RoI separation: $\Delta\eta, \Delta\phi \geq 0.2$
  - RoI resolution: $\sigma_\eta, \sigma_\phi < 0.1$
- Universal: suitable for e/γ, τ(h) and jets
- Explicit: encoding of RoI co-ordinates by ASIC
- Economical: no extra HW, built into CP ASIC
- Efficient: selects isolation with minimal leakage $\Rightarrow$ $\sim$1% drop in efficiency, but $\sim$10% drop in rate

Bunch-crossing Identification (BCID)

- Associates broad calorimeter pulses with single bunch-crossing (25 ns)
- Pipelined FIR filter plus peak-finder



- Constant pulse shape over E_T range *essential*
- Efficient down to 2 GeV; robust against timing jitter
- Saturated pulses assumed "flat top" $\Rightarrow$ count saturated samples to locate pulse max
- Pulses must retain rising and falling edges
- Non-zero pulses on alternate cycles $\Rightarrow$ BC multiplex two channels each two cycles

LVL1 Demonstrator Programme

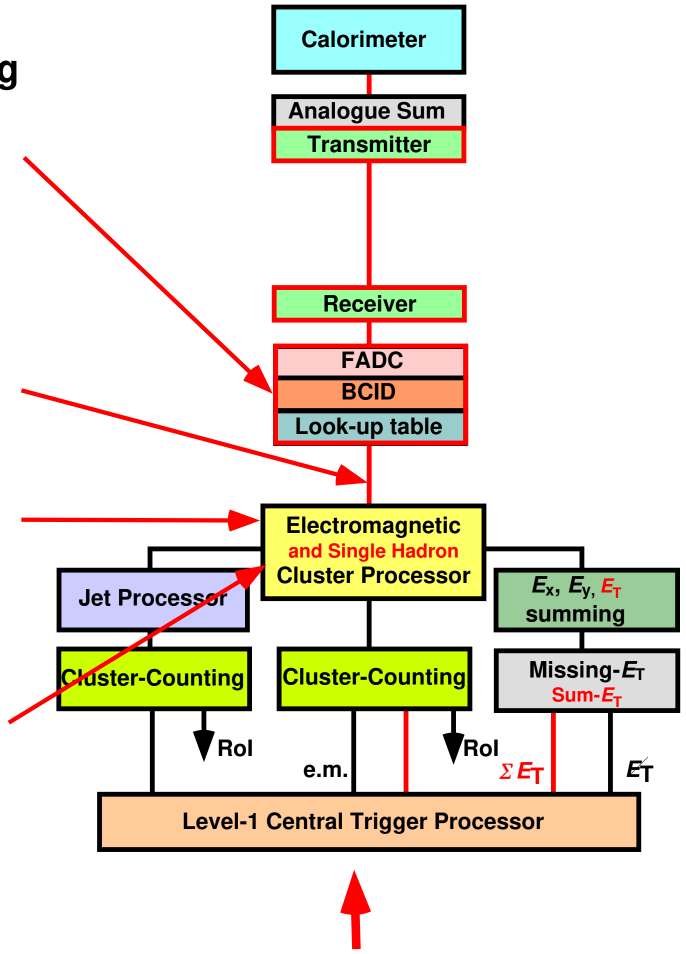
- Algorithm implementation demonstrated in testbeam 1993–95
- Data transmission technologies demonstrated 1996–98

1995
Efficient bunch-crossing identification (BCID) at 40 MHz

1996
Electrical (& optical) links run at 800 & tested at 1600 Mbaud

1994
E.M. cluster-finding in pipelined 40 MHz ASIC

1996
Multiplexing ASIC sending & receiving data at 160 Mbit/s

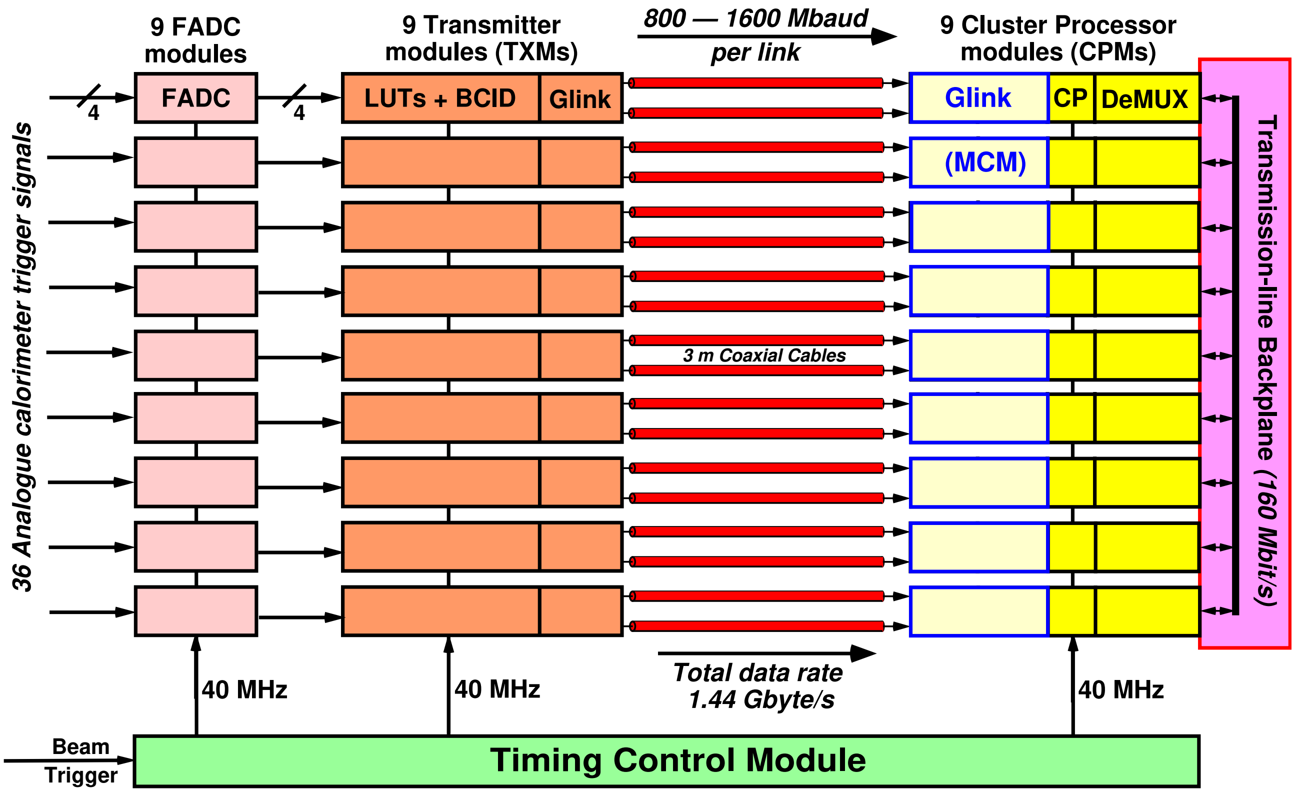


1997
Whole slice tested:
TileCal-FADC-TXM-CPM-JPM-CTPD
CP Backplane transmission &timing

- Design optimisation ⇒greater robustness

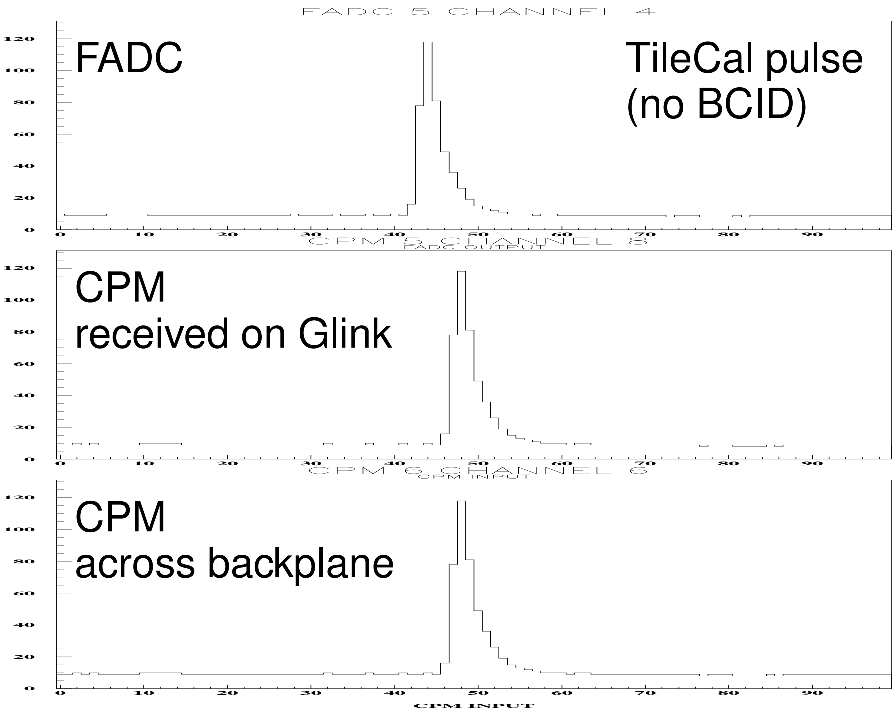
1997/98 CP Demonstrator

- Set-up:
  - 9 FADC/TXM/CPM chains
  - 18 Glinks in total
  - 36 TileCal towers
  - Each CPM reads 21/25 towers from backplane



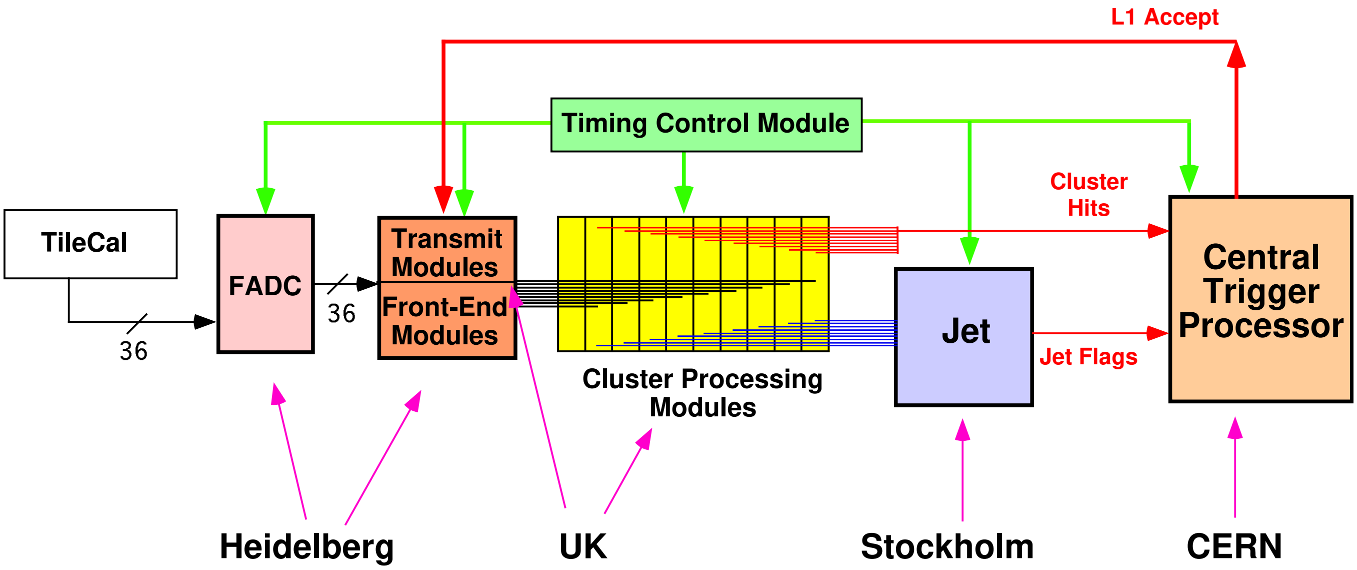
- Test Glinks in “real” environment
- Test inter-CPM fan-out via 160 Mbit/s backplane
- Timing strategy investigated
- Data integrity measured ⇒BER tester

GLINK and Backplane transmission



1997/98 LVL1 Slice tests

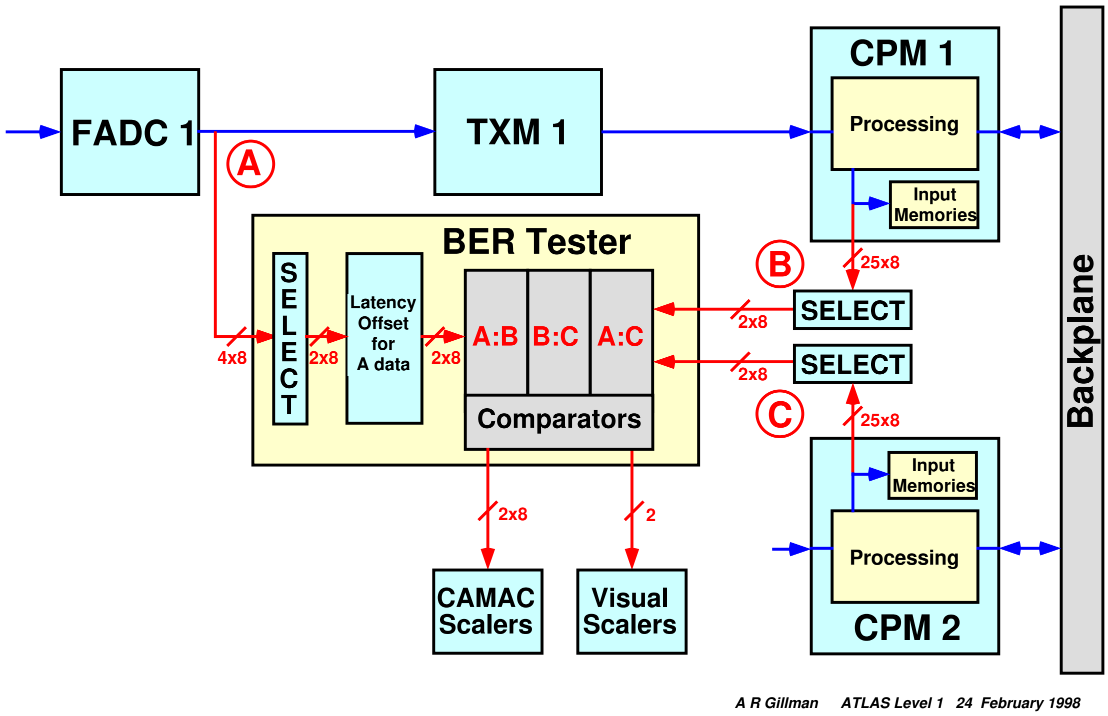
- Establish CPM communication with CTP
- Test CTP and response to LVL1 accept
- Test of FPGA for jet processing



BER testing

- Calorimeter pulses too clean to test for cross-talk
- White noise provides more realistic data:
  Uncorrelated channel-to-channel on Glinks, CPMs
- Custom BER test system built

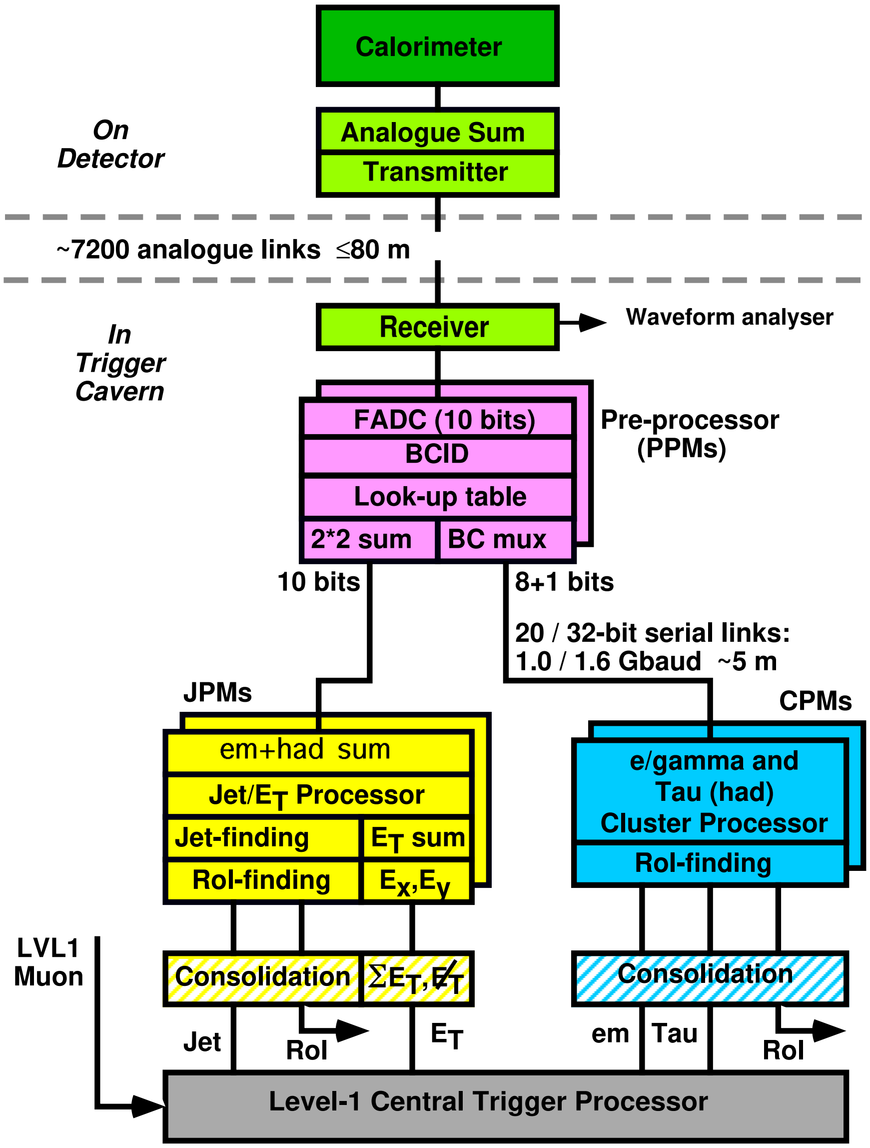
Bit-error Rate Measurement System



- BER $< 10^{-13}$ across Glink *and* backplane
  (no real errors yet observed)
- Glink cables ok up to 5 m, even at 1600 Mbaud

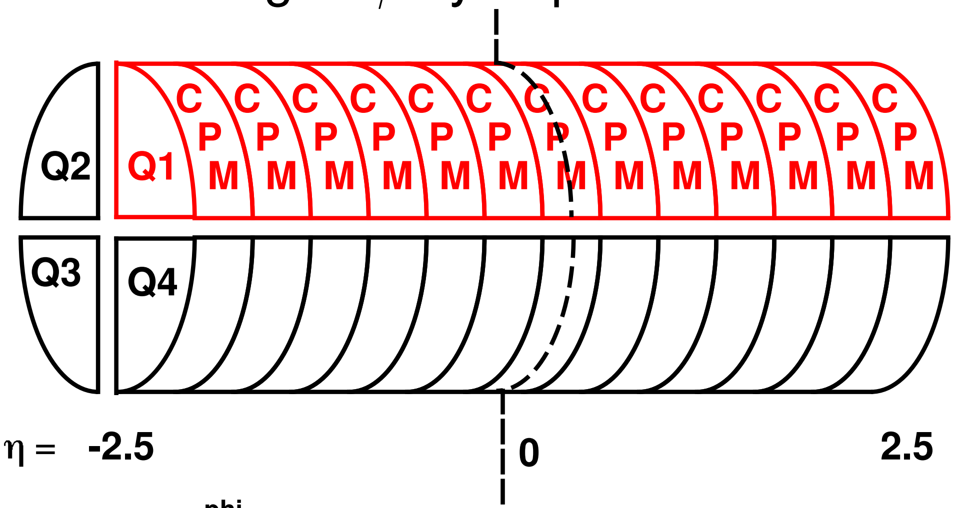
CP Architecture

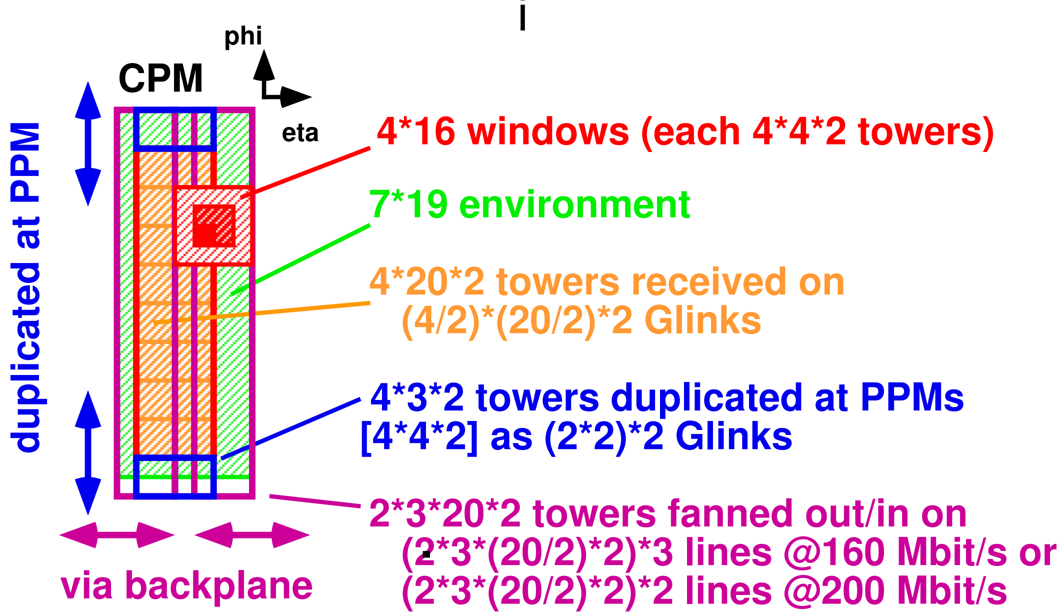
- Simpler organisation of CP system
- Jet/E_T inputs directly from PPMs; reduces CP I/O
- Bunch-crossing multiplexing of trigger towers
- Error detection integral across Glink/backplane



Phi-quad CP system

- Phi-quadrant crates, 13 CPMs over $|\eta| < 2.5$
- Each CPM spans whole quadrant in ϕ
- Inter-CPM sharing in η by backplane fan-out
- Inter-CPM sharing in ϕ by duplication at PPM

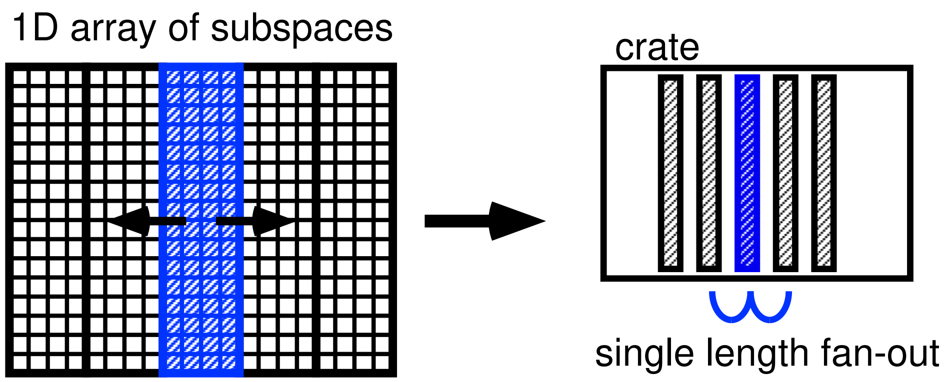


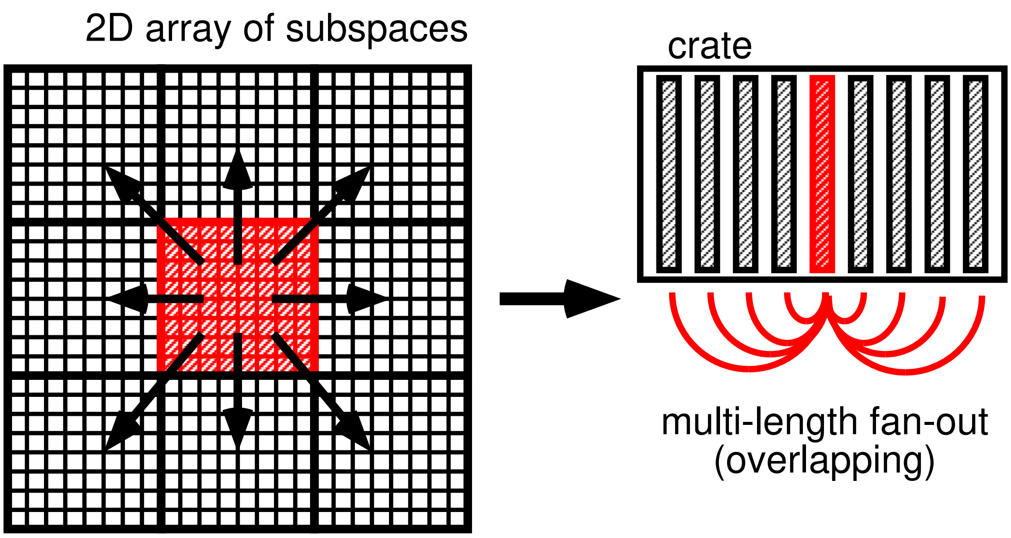


- BC mux reduces pin-count $\Rightarrow$fan-out of pairs in ϕ
- Glinks power-hungry; low-power link desirable

1D fan-out

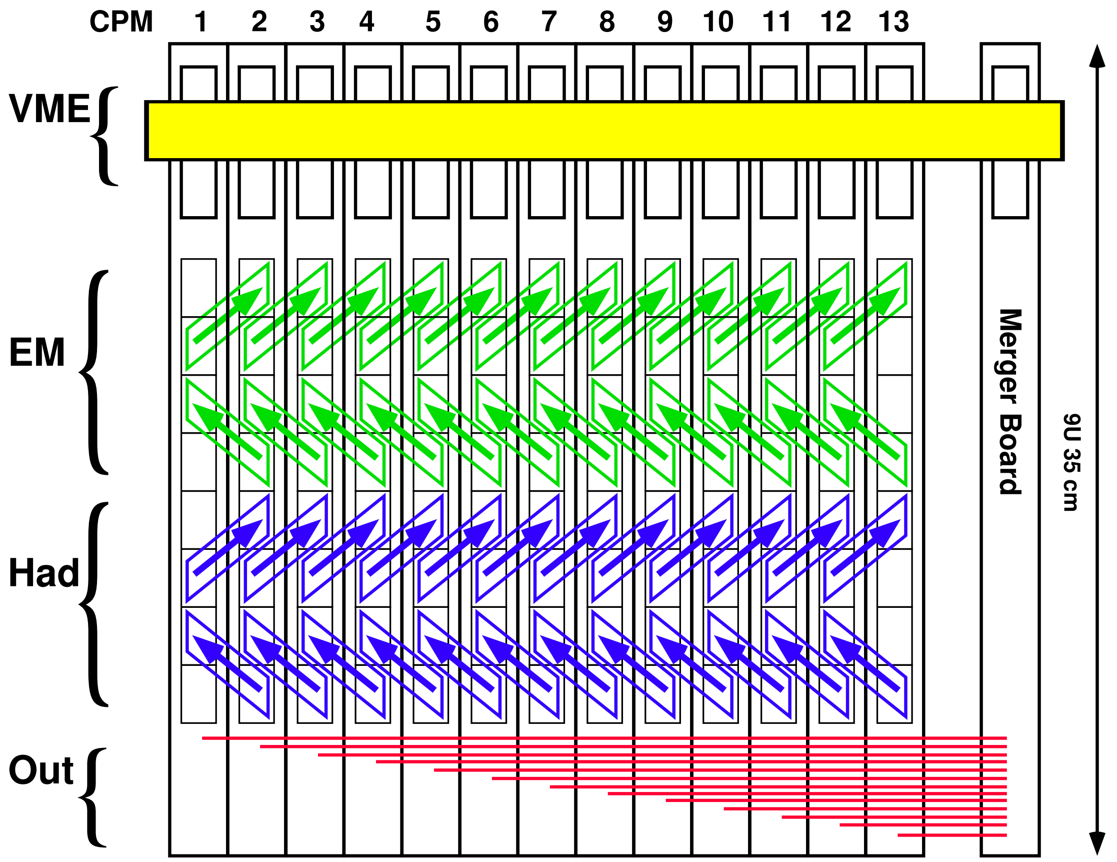
- Crate of modules maps 1D array of subspaces
- Physical layout (crate/module) $\equiv$ Logical layout (quadrant/subspace)
- Each CPM communicates with only 2 neighbours
- Much simpler than 2D array within same crate (2D backplane in demonstrator programme)





Simpler CP backplane

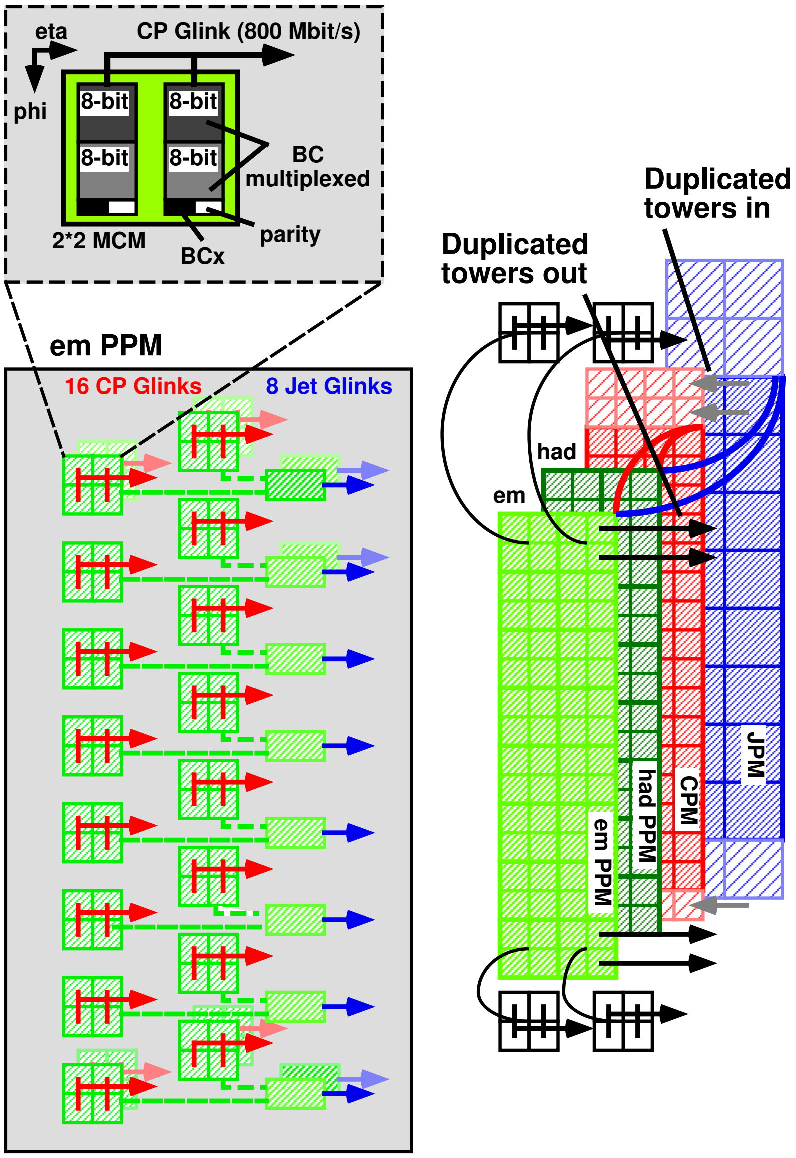
- Each CPM communicates with only 2 neighbours:
  - Shorter backplane paths of uniform length
  - Simpler timing, all CPM pairs same phase difference
  - Simpler geometry, single layer design possible
  - Improved grounding
  - ⇒Better noise performance, higher speed ?



- PPM em/had separation maintained on backplane
- Trigger sums on backplane to merger board, combined and transmitted to CTP

PPM–CPM/JPM mapping

- PPMs are em-only or had-only
- PPM, CPM and JPM all cover same-size region
- Summing of Jet/E_T inputs groups towers as 2*2
- BC mux $\Rightarrow$2*2 towers + error detection on Glink
- Inter-crate sharing by link duplication at PPM



Summary and conclusions

- New decluster/RoI algorithm within CP ASIC
- Suitable for all algorithms: e/γ/τ *and* jets
- Algorithm studies almost complete for TPTP
- Demonstrator programme (almost) completed
- Multi-CPM system tested with TileCal Oct '97
- Multiple Glinks robust at 800 Mbaud over $>$5m
- Backplane transmission at 160 Mbit/s successful
- BER across Glink/backplane $< 10^{-13}$ (zero real errors)
- Complete slice: FADC-TXM-CPM-JPM-CTPD
- New phi-quad CP architecture: simpler backplane $\Rightarrow$easier timing, less cross-talk, faster ?
- Bunch-crossing multiplexing reduces pin-count
- Error detection across serial link and backplane
- Inter-crate tower sharing by duplication at PPM
- Single PPM–CPM–JPM modularity $\Rightarrow$simpler organisation
- Focus on TDR for June 1998