Level-1 Calorimeter Trigger

Paul Bright-Thomas (Birmingham)

on behalf of

Birmingham, Heidelberg, Mainz,

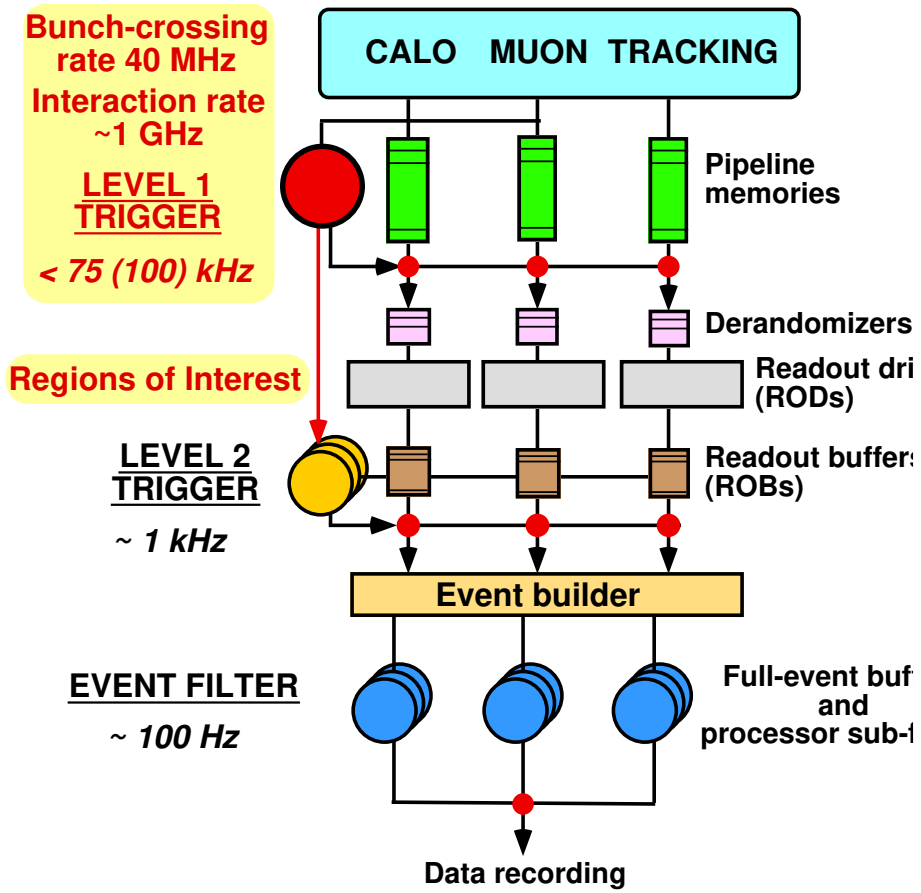
QMW (London), Rutherford, Stockholm

- ATLAS trigger overview
- Algorithms
- Trigger architecture
- Pre-processor
- Serial transmission
- Cluster processor
- Jet/Energy-sum processor
- Summary

ATLAS Trigger Overview

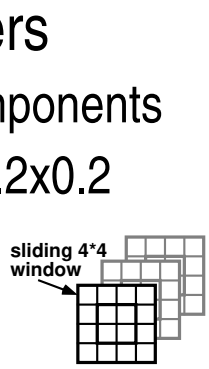
- Multi-level trigger

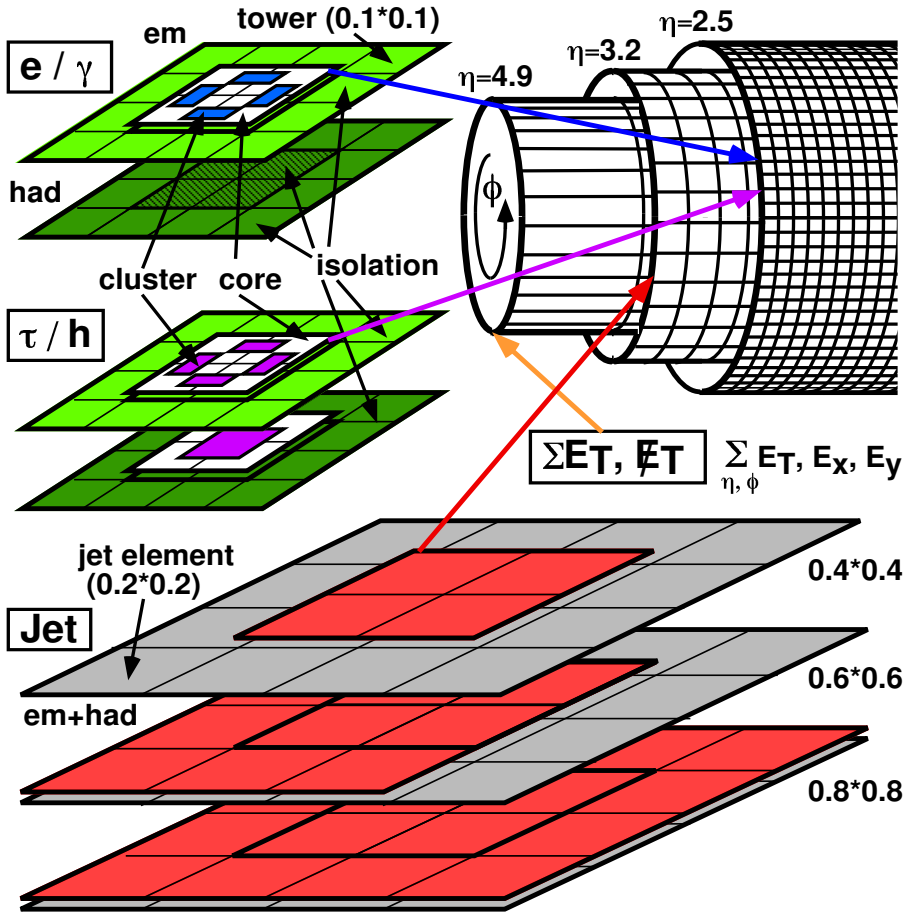
  40 MHz ⇨75 kHz ⇨1 kHz ⇨100 Hz
- Data front-end pipelined
  - Decision latency 2 μs
- Level-1
  - Calorimeter and Muon triggers
  - Central Trigger Processor
- Level-2
  - Full granularity data
  - Regions of Interest
- Event Filter -- full reconstruction



Calorimeter Trigger Algorithms I

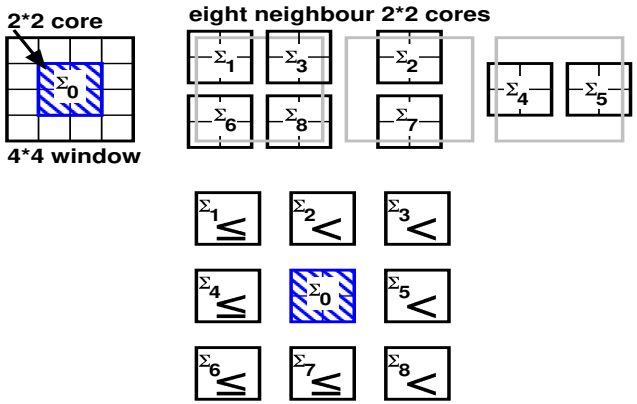
- Analogue trigger towers
  - Separate em/had components
  - $\Delta\phi x\Delta\eta$=0.1x0.1 or 0.2x0.2
- e/γ and τ/h clusters
  - Sliding windows
  - Isolation vetoes on em and had
- Jet clusters
  - Programmable cluster size
- Energy sums
  - ΣE_T ,E_t^{miss} out to $|\eta|<4.9$
- Discriminate at 8 E_T thresholds
- Cluster/jet multiplicity to CTP

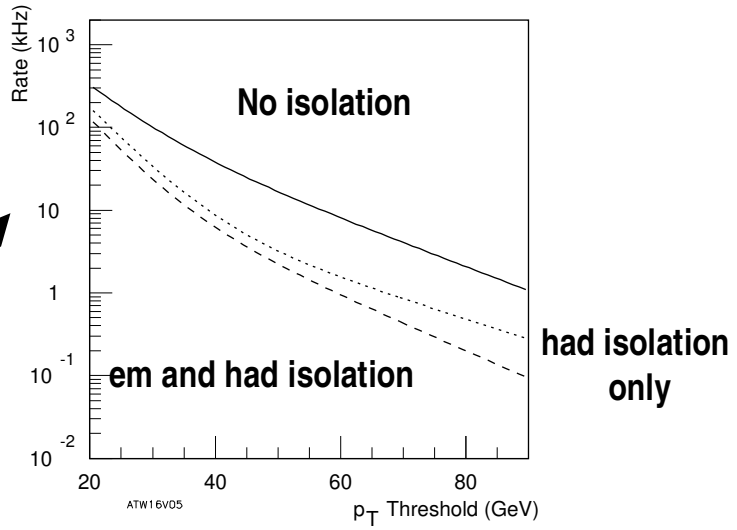




Calorimeter Trigger Algorithms II

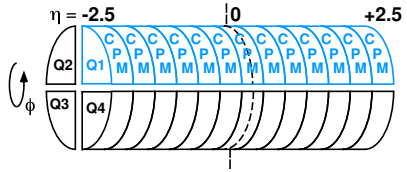
- Declustering
  - Integral within windows
  - Require local E_T maximum
  - Identifies RoI co-ordinate
- Versatile e/γ-τ/h thresholds
- Saturation flagged to Level-2
- FCAL towers for “forward jets”… ?
- Flexible implementation in FPGAs
  - Further algorithmic refinement
- Performance
  - separate em and had isolation vetoes reduce rates

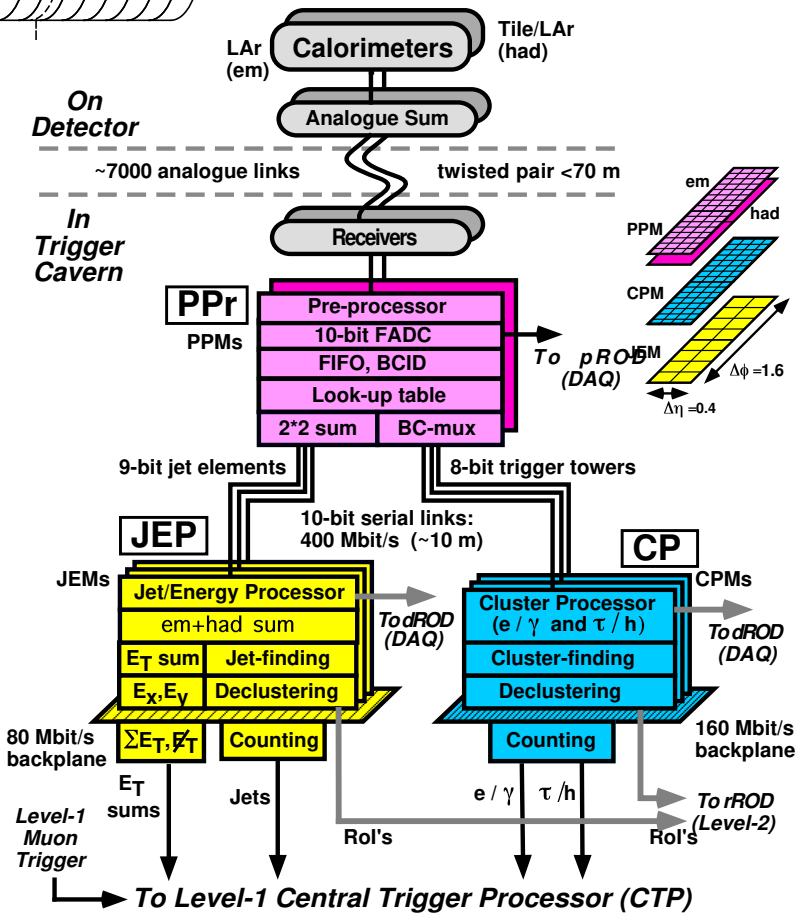




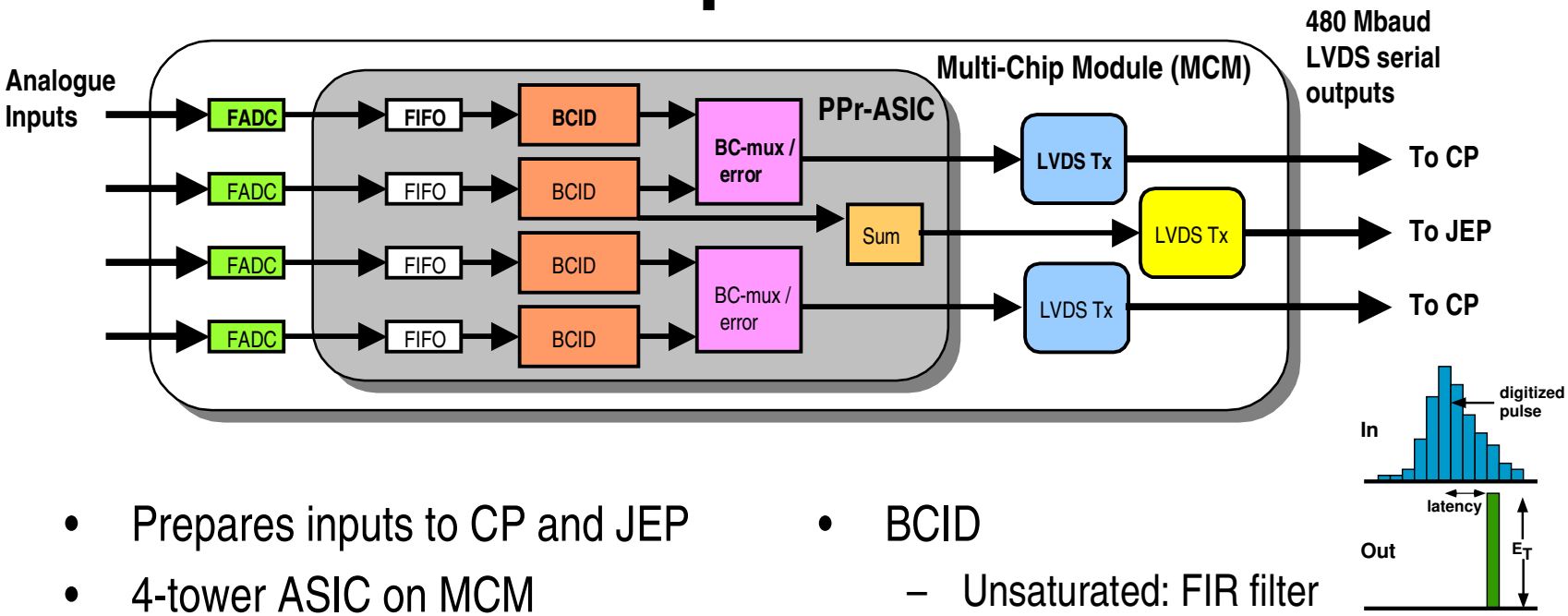
Calorimeter Trigger Architecture

- Quadrant architecture
  - Module crate mapped to 1D array
  - Common modularity, simpler data-flows
- Data sharing between windows/devices
  - High bandwidth fan-in/fan-out
  - Maximum density processors
- Pre-processor: prepares tower inputs
- Cluster Processor (CP): e/γ and τ/h
- Jet/Energy-sum Processor (JEP)
- Interfaces
  - Calorimeters: analogue pulses (70m)
  - CTP: feature multiplicities at 40 MHz
  - Level-2: trigger features RoIs
  - DAQ: inputs/results read-out after L1A





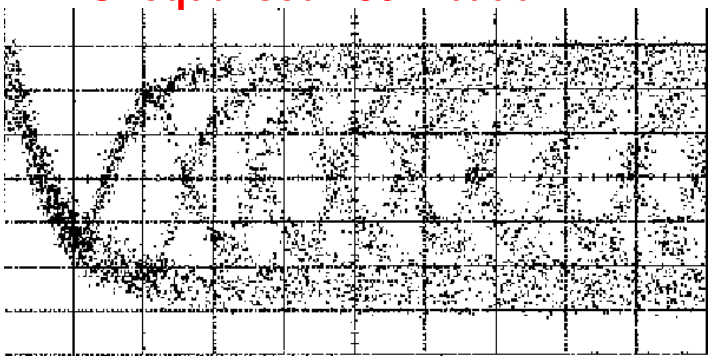
Pre-processor



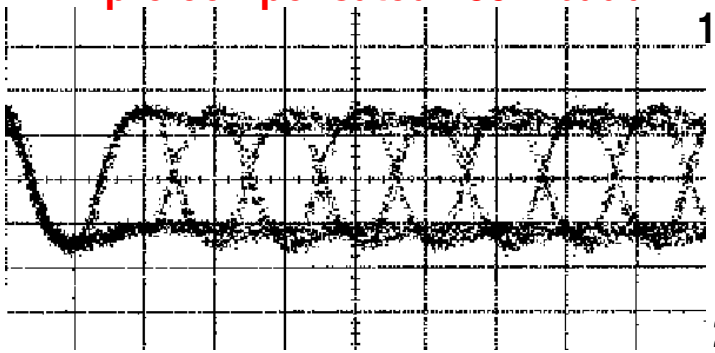
- Prepares inputs to CP and JEP
- 4-tower ASIC on MCM
  - 64 towers per PPM (em or had)
- Digitisation: 12 bits at 40 MHz
- Synchronisation
  - Coarse: FIFOs
  - Fine: ADC strobe (Phos4)
- BCID
  - Unsaturated: FIR filter
  - Saturated: Edge-discrimination
  - External: Analogue (backup)
- Jet/Energy input summation
- Serial transmission ⇨
- Pipeline readout to DAQ

Serial Transmission

Unequalised 480 Mbaud



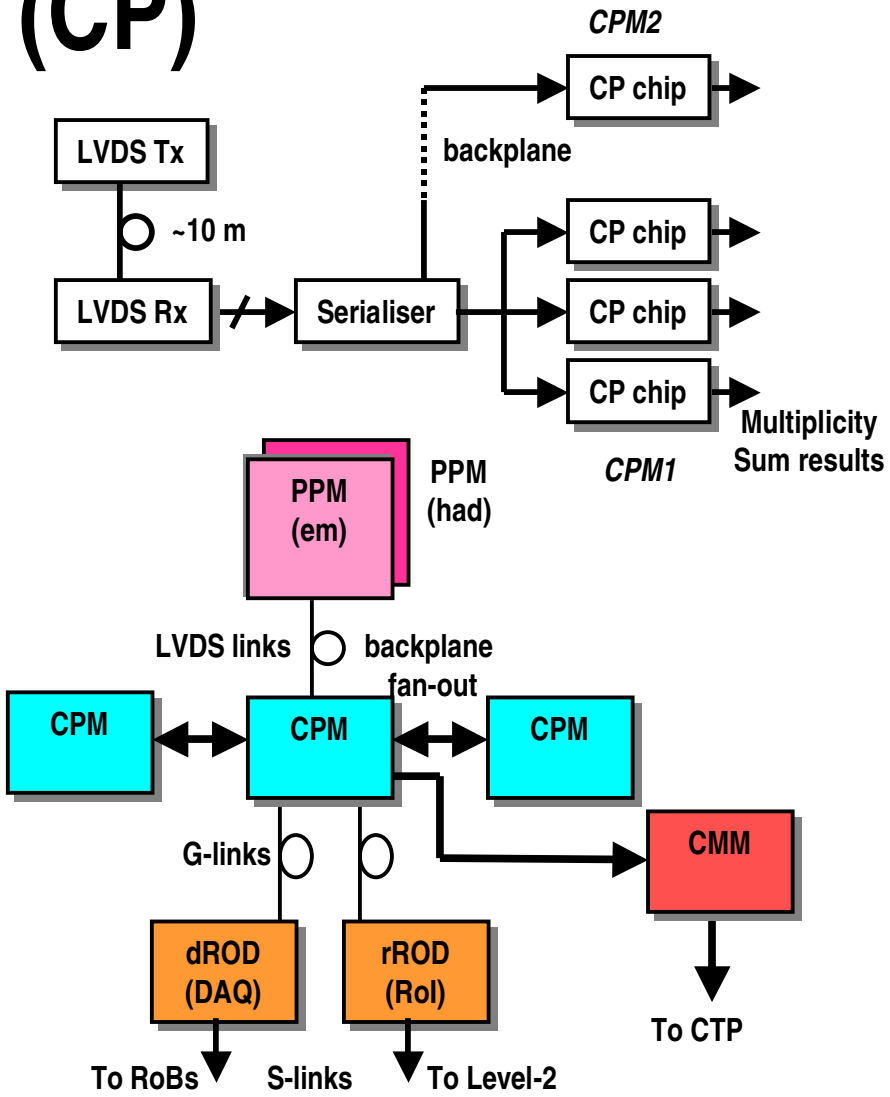
RL pre-compensated 480 Mbaud



- LVDS
  - 400 Mbit/s differential
  - Low power, <150 mW per end
  - Cable compensation required
  - Bit-error rate < 10^{-13} up to 15m
- BC-multiplexing
  - Empty cycle follows BCID result
  - 2 towers interleaved per channel
- Error protection
  - Parity across links and backplane
  - Suppression of error-prone links
- Compact cabling + connectors
  - Backplane entry routing
- H-P Glink for DAQ/RoI read-out

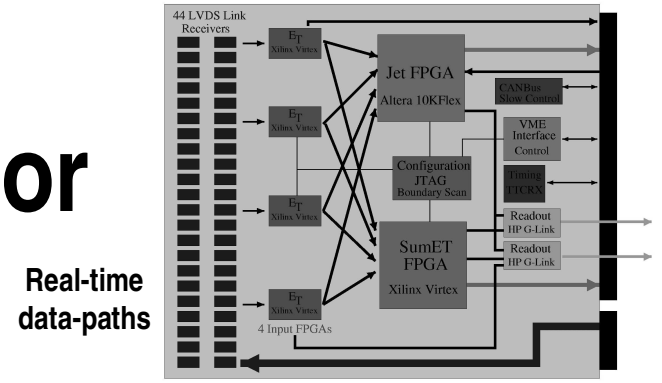
Cluster Processor (CP)

- Performs e/γ and τ/h algorithms
- CPM processes 64 windows
  - 80 LVDS, 20 Serialisers, 8 CP chips
- Serialiser FPGAs
  - Parallel LVDS output re-serialised for backplane fan-out at 160 Mbit/s
- CP chip FPGAs
  - 8 windows, 16 thresholds
  - Programmable logic gives flexibility
- Common RODs
  - For both DAQ and RoI read-out
  - Read-out via G-links
  - Data formatting in FPGAs

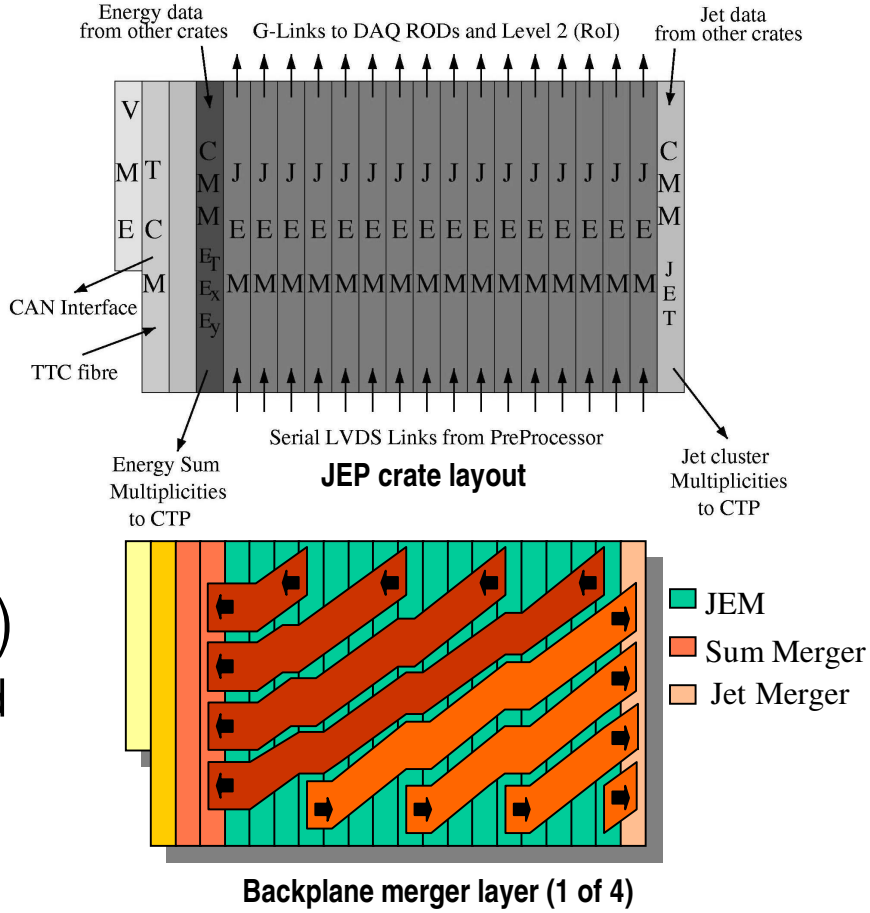


Jet/Energy-sum Processor

- Jet and Sum FPGAs
  - JEM processes 32 jet windows
  - Programmable logic
  - Adapt for forward jets
- Common CP/JEP backplane
  - Fan-out/fan-in (160 or 80 Mbit/s)
  - Merging of results
  - Incoming LVDS tower data
  - VME, timing and DCS
- Common Merger Module (CMM)
  - Multiplicity sums at each threshold
  - Global sums of E_x ,E_y and E_T
  - Crate-merging via backplane



Real-time data-paths



Backplane merger layer (1 of 4)

Summary

- Level-1 triggering of isolated e/γ, τ/h, jets and ΣE_T ,E_T^{miss}
- Algorithms thoroughly studied
  - Enhancements for robustness and simplicity
  - Further refinement possible due to CP/Jet/Sum FPGAs
- Coherent architecture, common components
- Appropriate technologies identified/verified
- Many component PDRs completed, FDRs begun
- Software development in progress
  - Online SW using DAQ-1 framework
  - Offline SW and simulation design for new ATLAS framework
- Full-function prototypes mid-2001…multi-system slice tests