The Final Multi–Chip Module of the ATLAS Level–1 Calorimeter Trigger Pre–Processor

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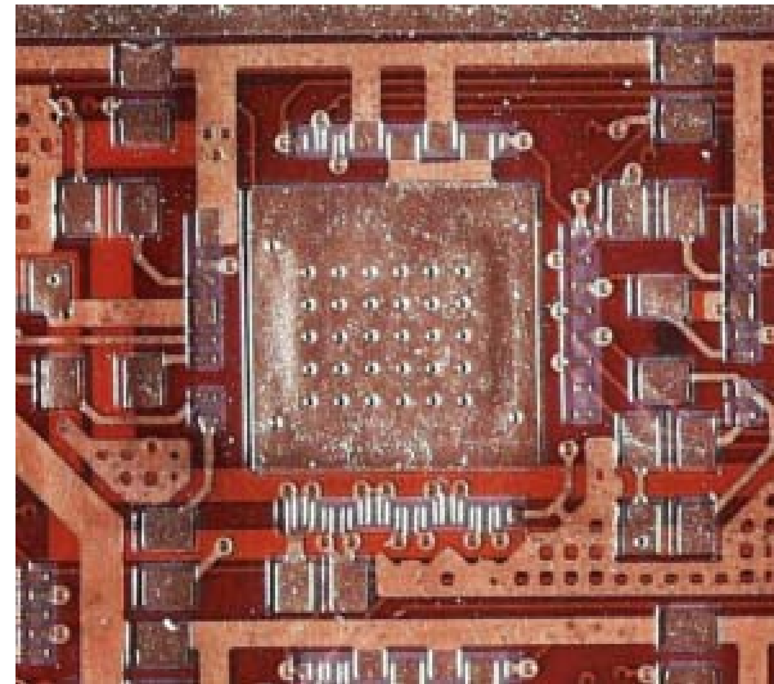
- Summary



detail of the MCM substrate

Summary

Requirements for the ATLAS Level–1 Trigger:

– pipelined signal processing at 40 MHz for 7200 analog signals
and trigger readout at 100 kHz

– Pre–Processing in 400 ns requires ASIC and MCM technologies
and reduces the system size to 8 crates

Multi–Chip Module:

– MCM is the key component,
all trigger data pass it before any event can be accepted

– A demonstrator MCM was successfully designed, simulated, and operated

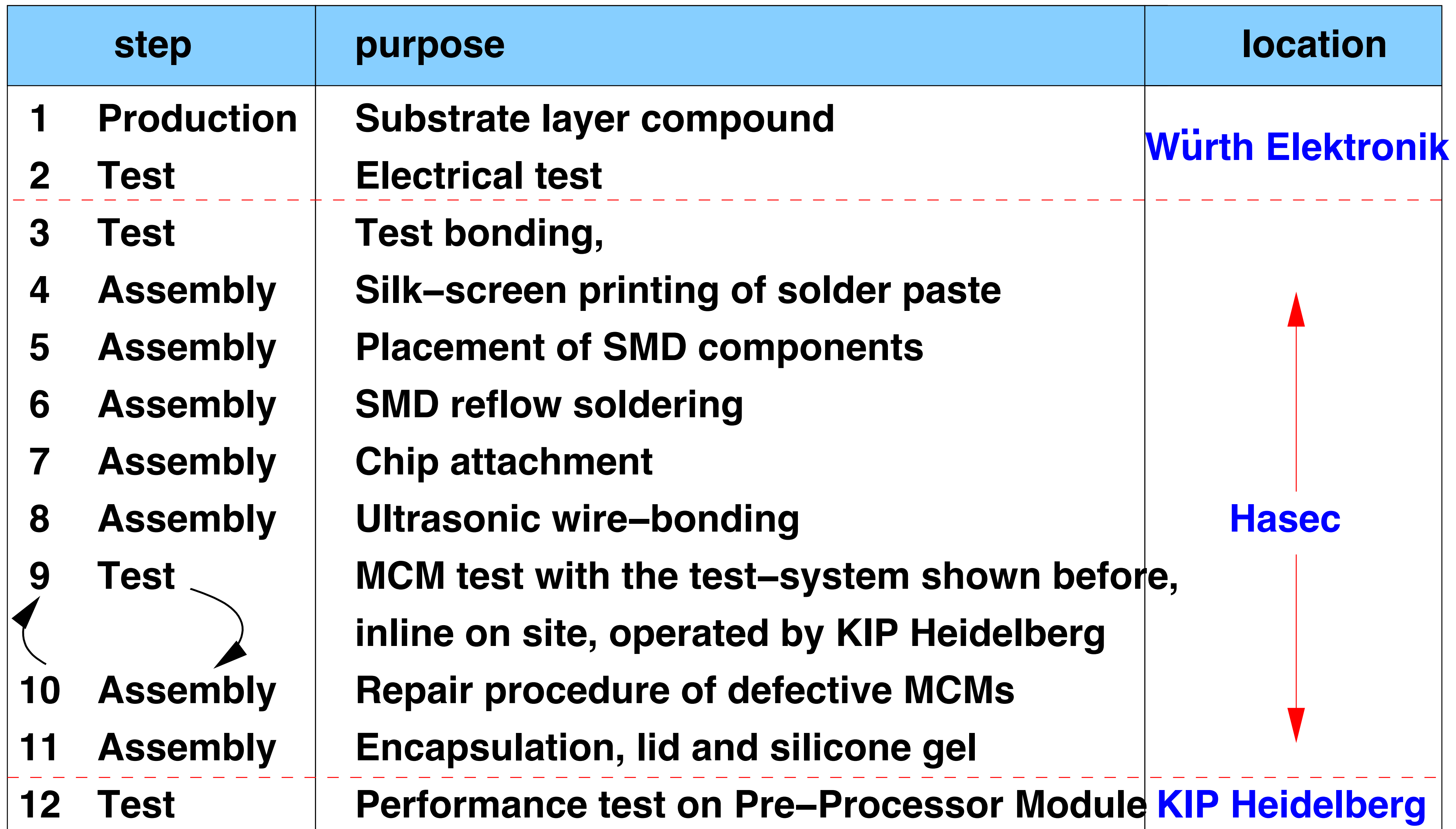
Final production for ATLAS:

– the design of the final MCM is finished

– a pre series of 100 MCM will be produced in the end of 2001

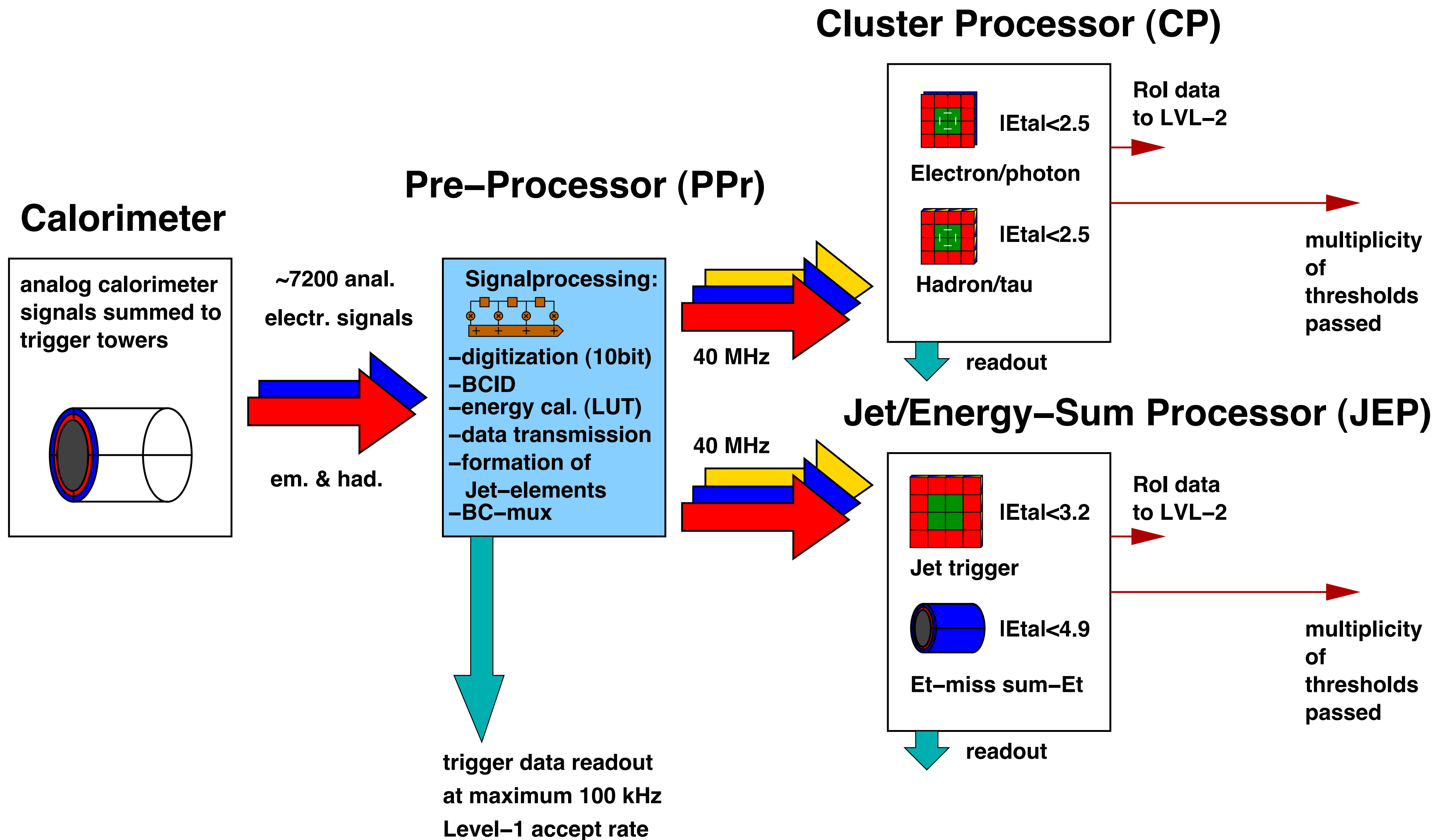
Sequence for mass production and quality assurance

Mass production is done in cooperation with industry (Würth Elektronik + Hasec)



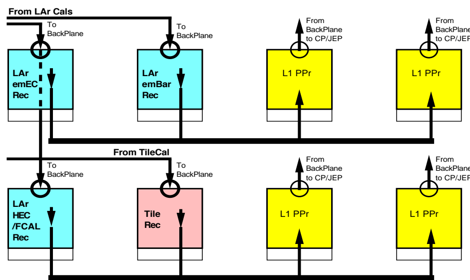
step		purpose	location
1	Production	Substrate layer compound	Würth Elektronik
2	Test	Electrical test	
3	Test	Test bonding,	Hasec
4	Assembly	Silk–screen printing of solder paste	
5	Assembly	Placement of SMD components	
6	Assembly	SMD reflow soldering	
7	Assembly	Chip attachment	
8	Assembly	Ultrasonic wire–bonding	
9	Test	MCM test with the test–system shown before, inline on site, operated by KIP Heidelberg	
10	Assembly	Repair procedure of defective MCMs	
11	Assembly	Encapsulation, lid and silicone gel	
12	Test	Performance test on Pre–Processor Module	KIP Heidelberg

ATLAS Calorimeter Trigger Architecture



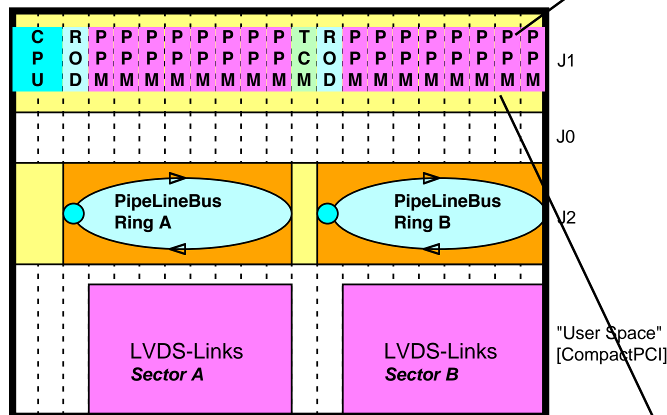
Pre–Processor System

8 crates



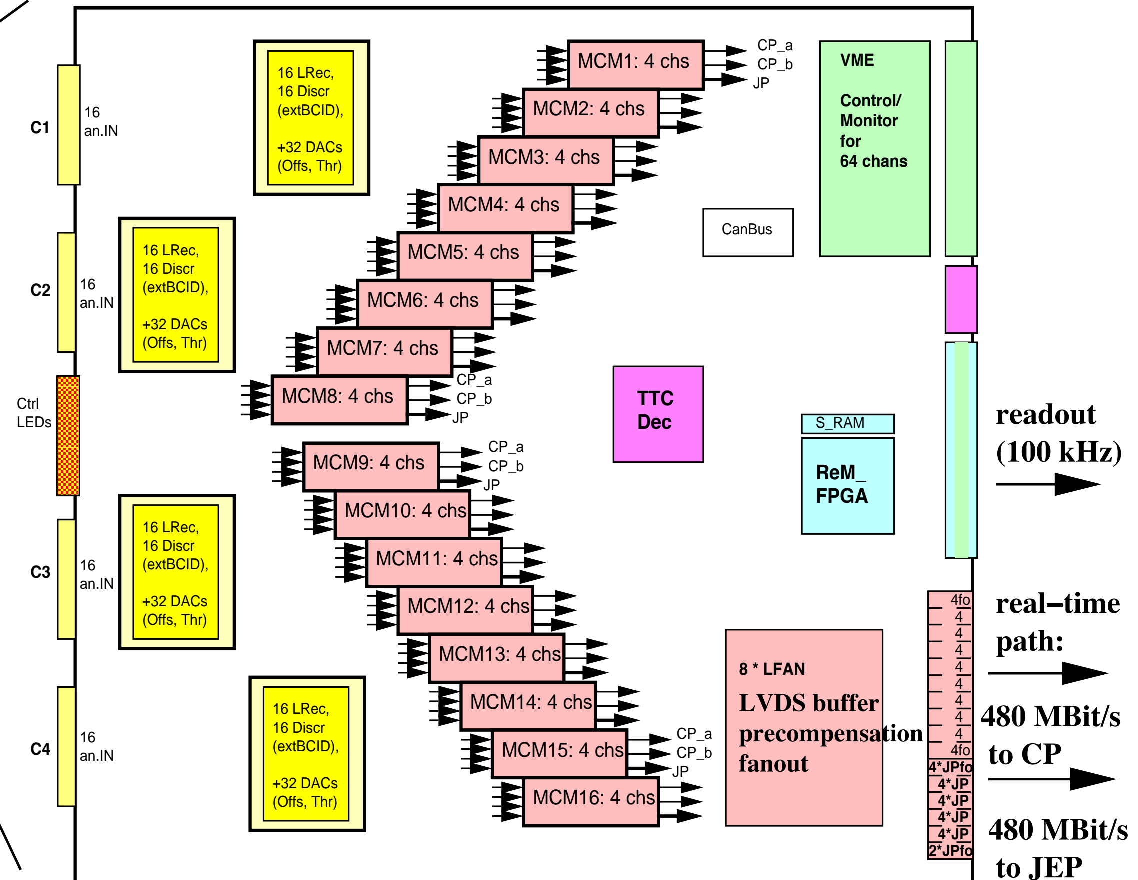
In each crate:

9u VME64x Crate with PipeLineBus on "user-defined" J2-pins



- 2 Read–Out Driver Modules
- 1 VMEbus Crate Controller
- 1 Timing and Control Module
- 16 Pre–Processor Modules

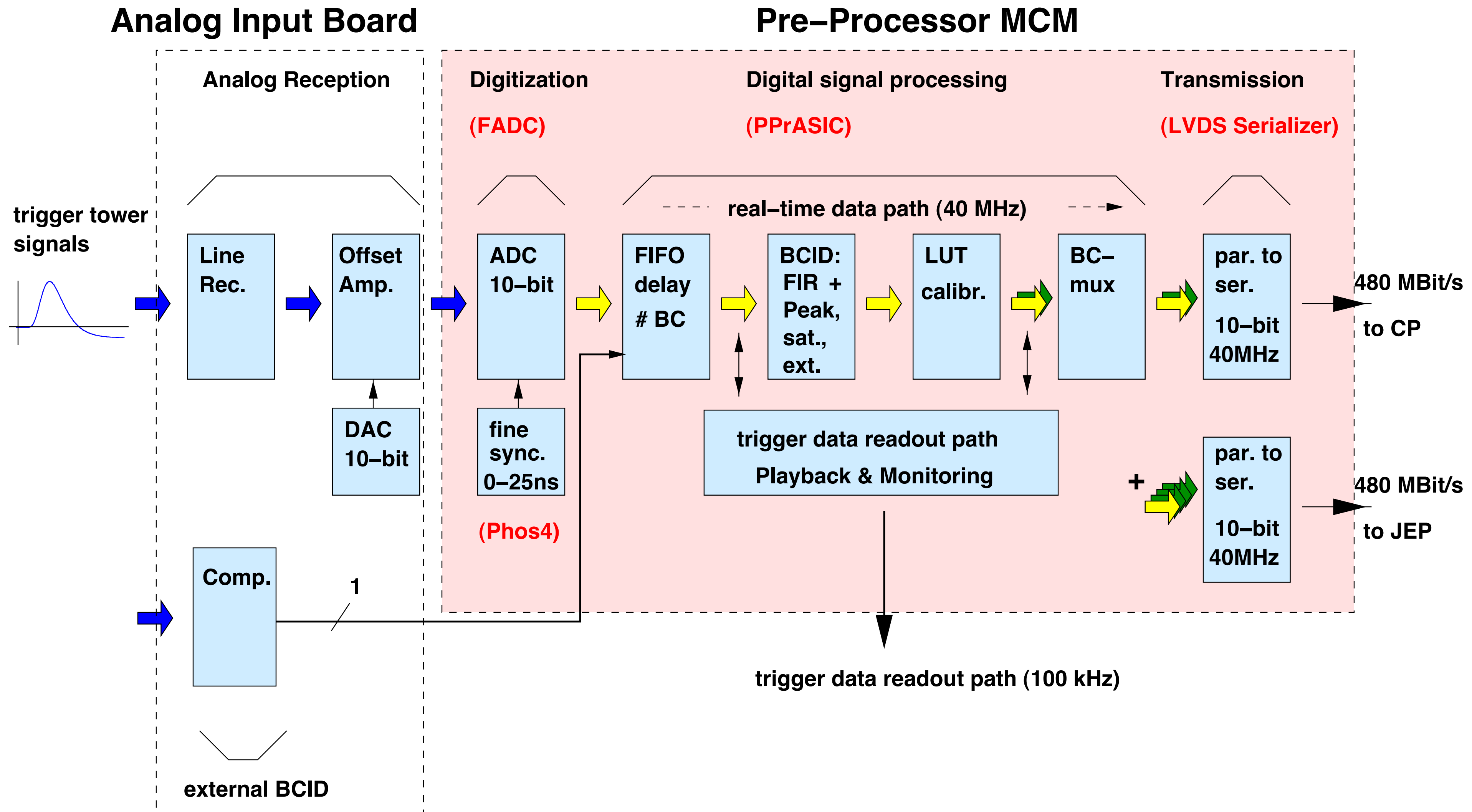
Pre-Processor Module



W. Hinderer

Preprocessing of Trigger Tower Signals

Four such channels are combined on one MCM:



MCM technology overview

TwinFlex® Würth Elektronik - Germany

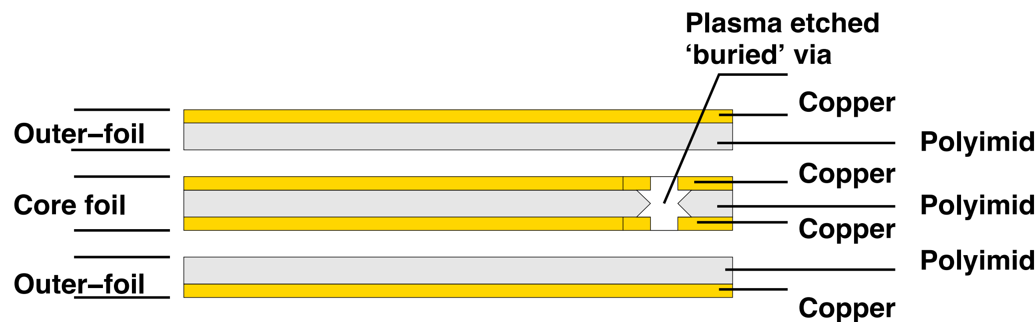
Layer structure: four−layer Cu-polyimide structure

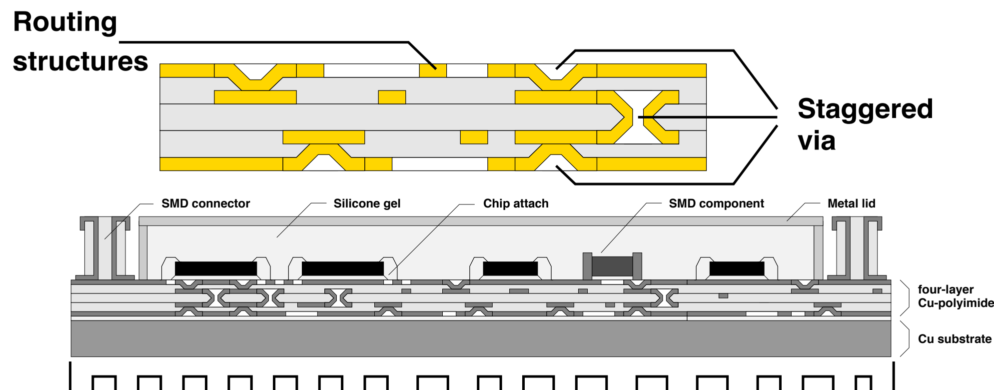
Substrate: electrically−isolated 0.8 μm Cu substrate

ATLAS constraints

Heatsink: 8 mm AL heatsink

Encapsulation: embedded silicone gel and metal lid





MCM Layout Properties as produced

– analog and digital parts were separated:
this applies to power and ground, the signal routing and the placement of the dies

– broad power traces (> 500μm) were used to limit the voltage drop,
the width of the other traces is usually only 100 μm

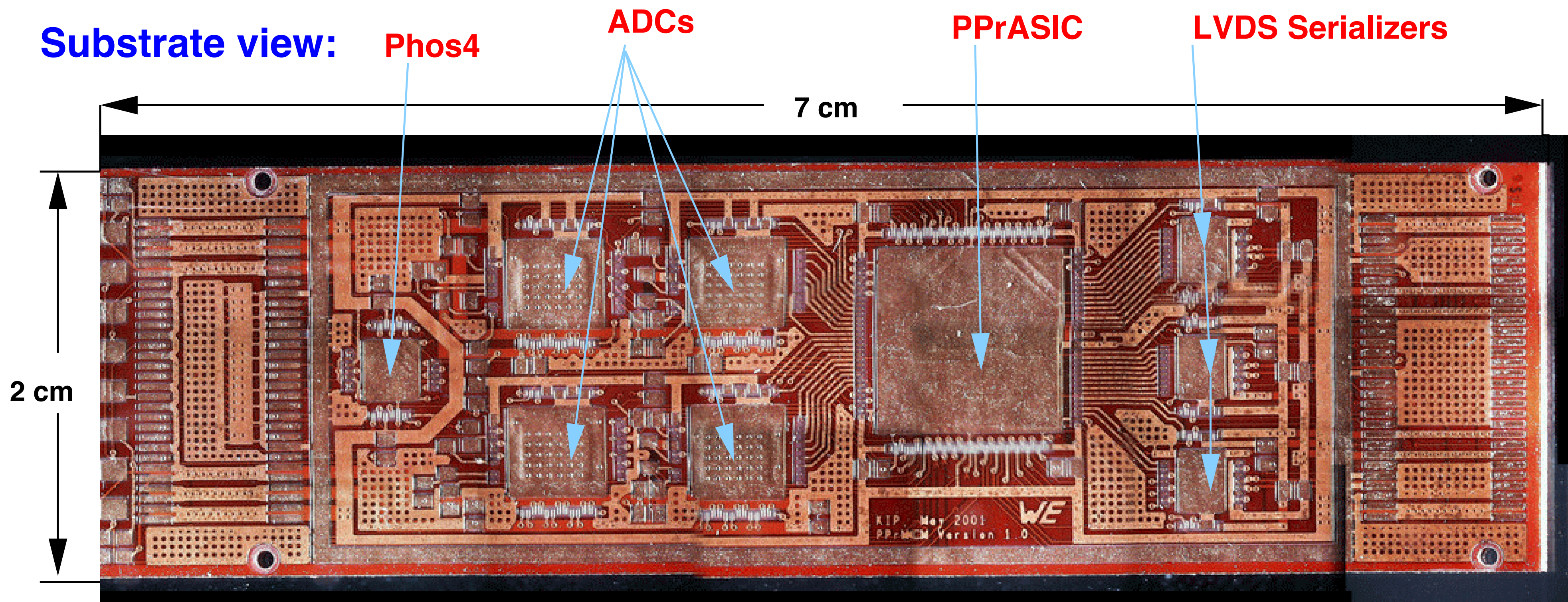
– for each die at least two decoupling capacitors were used

– due to the high power dissipation of the ADCs (~0.6 W for each),
thermal vias (staggered vias) were used to provide
good thermal conductance to the substrate

– EMI shielding by the ground layer and the cross–hatched shape
on the top layer

Final Multi–Chip Module

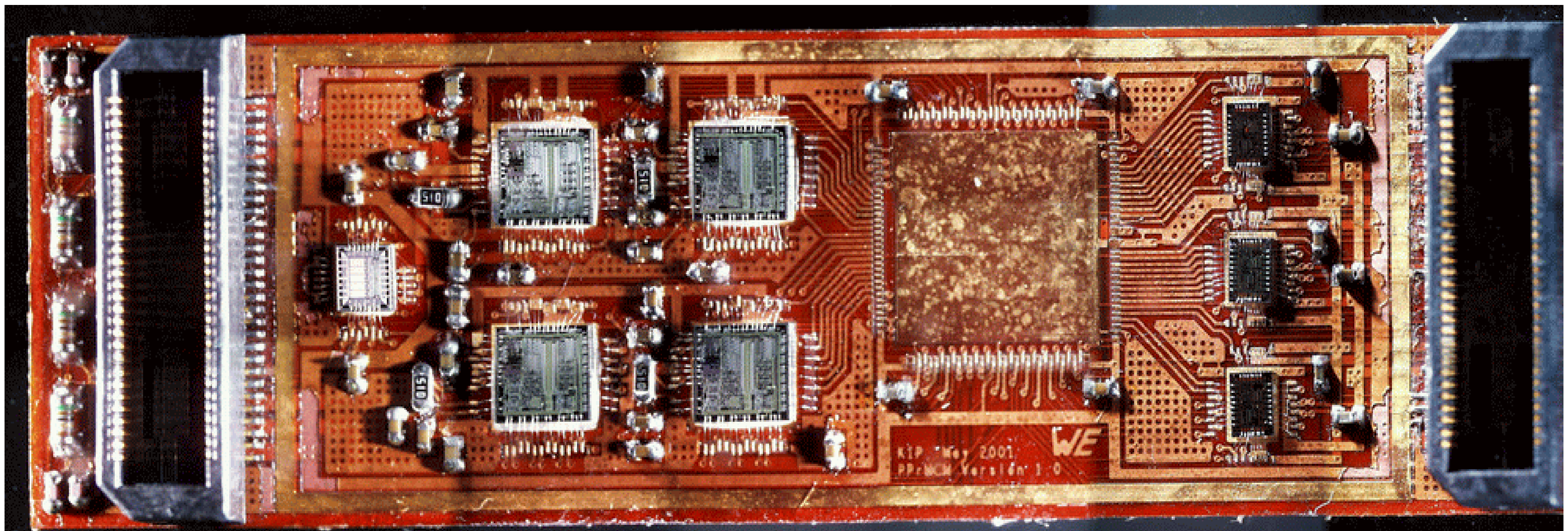
- pre–series of 6 Multi–Chip Modules was manufactured by Würth Elektronik
- considerable design experience has been gained from a demonstrator MCM
- 3 Multi–Chip Modules were partly assembled in the ASIC–Lab of Heidelberg
- 16 MCMs / Pre–Processor Module
- 3200 MCMs (including spares) are needed



Final Multi–Chip Module

- 9 dies: 3 LVDS Serializers (DS92LV1021, National Semiconductor), 4 ADCs (AD9042, Analog Devices), 1 Phos4 (CERN Microelectronics group), 1 PPrASIC (ASIC–Lab, University of Heidelberg)
- 2 connectors (BTH030) from Samtec
- 36 capacitors (size: 0402) and 8 resistors (size: 0603 and 0805)

Partly Assembled:

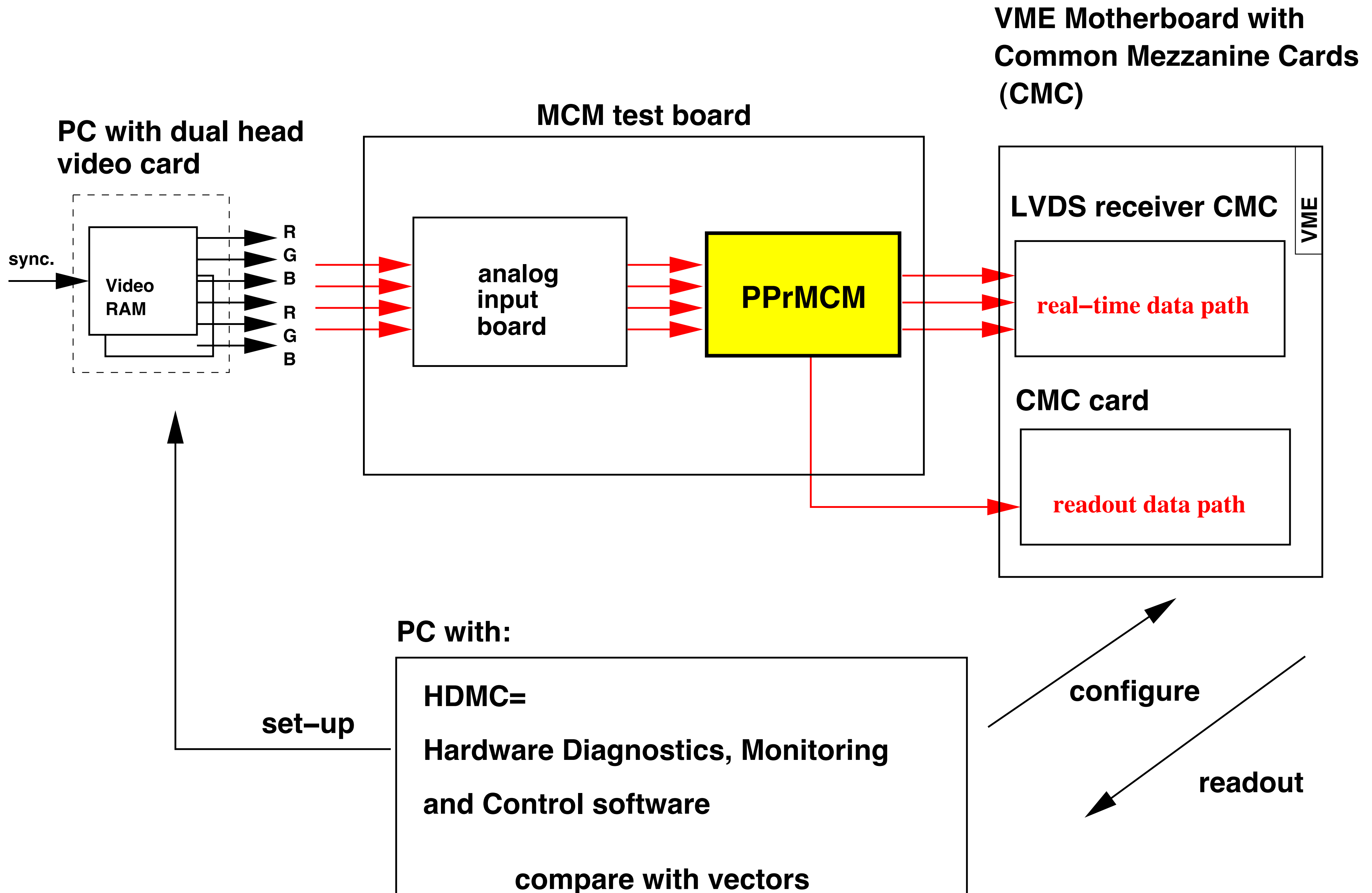


MCM Layout Properties

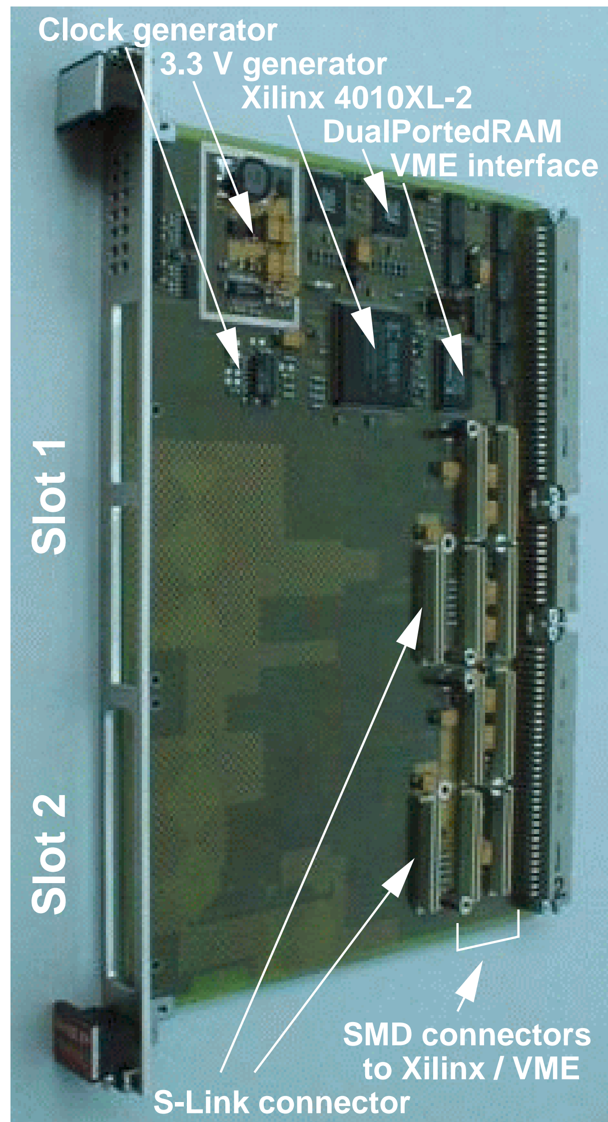
Layout properties

Property	Value
Feature size (Line pitch)	100 μm
Substrate dimension	2 cm x 7 cm
Total line length	~2.5 m
Ratio Silicon / Substrate	~11 %
Die count	9
Number of layers	4
Substrate thickness	1070 μm
SMD connector pins	120
Connector height	5 mm
Heatsink thickness	8 mm
Wire–bonds (AL)	~417
Wire–bond thickness	30 μm
Vias	932
Thermal Vias	120
Total power consumption	~5.2 W

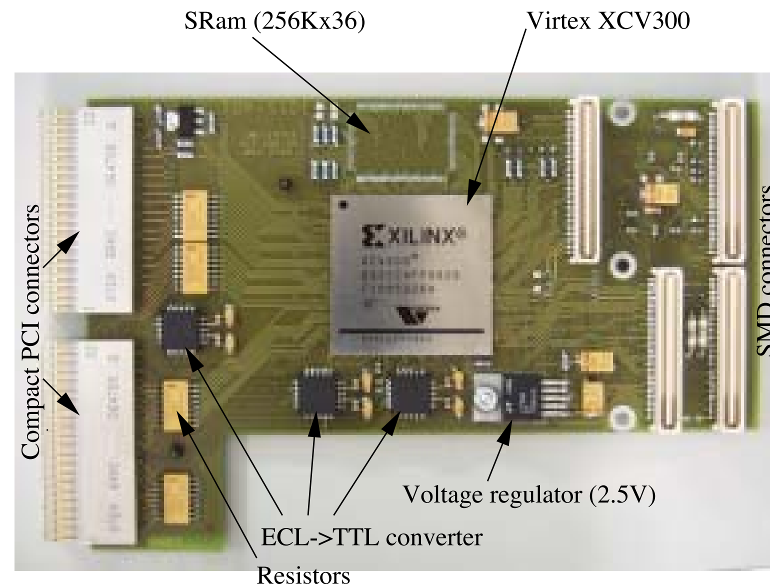
MCM Test Setup



Test Boards



VME motherboard



CMC daughtercard