ATLAS Level-1 Calorimeter Trigger: Subsystem Tests of a Prototype Cluster Processor Module

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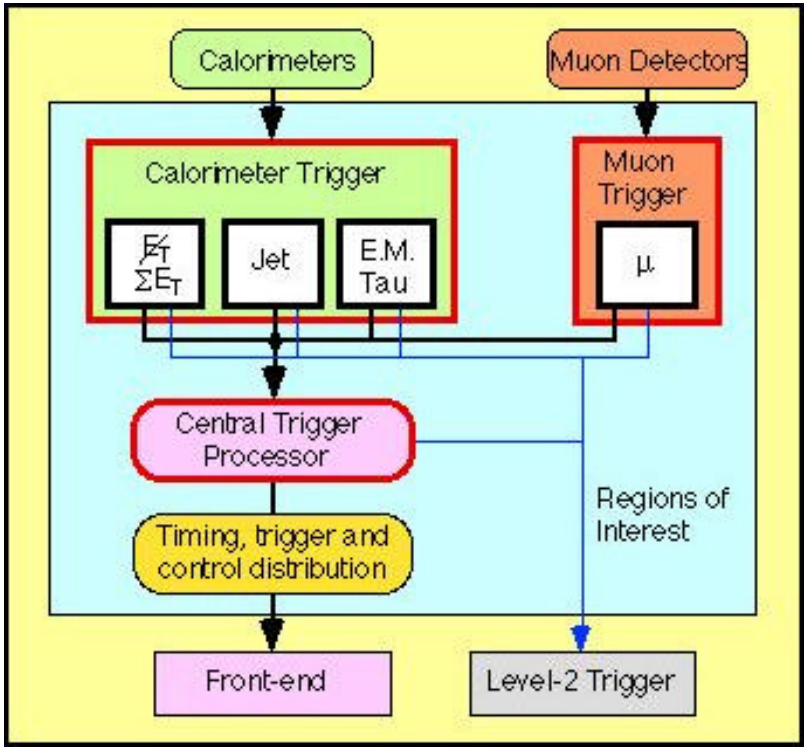
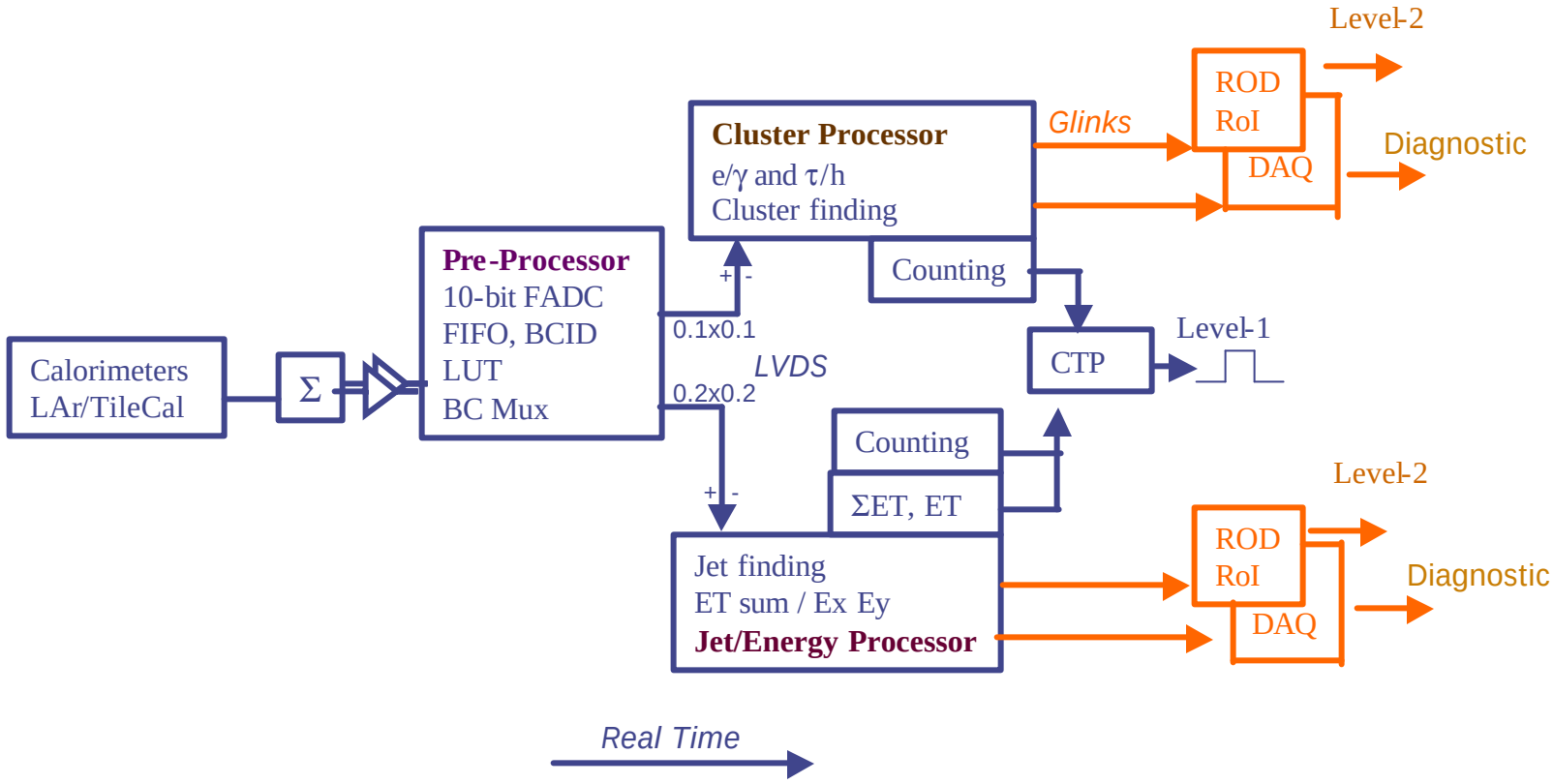
ATLAS Level-1 Calorimeter Trigger System

Level -1 Trigger Requirements

- Reduce 1 GHz interaction rate to a 75 kHz trigger rate
- Provide trigger multiplicity information to the CTP:
  - e/γ and τ/hadron
  - jets
  - missing and total ET
  - muons (separate trigger)
- Provide Region of Interest (RoI) information to the Level-2 trigger system
- Provide data for monitoring and diagnostics

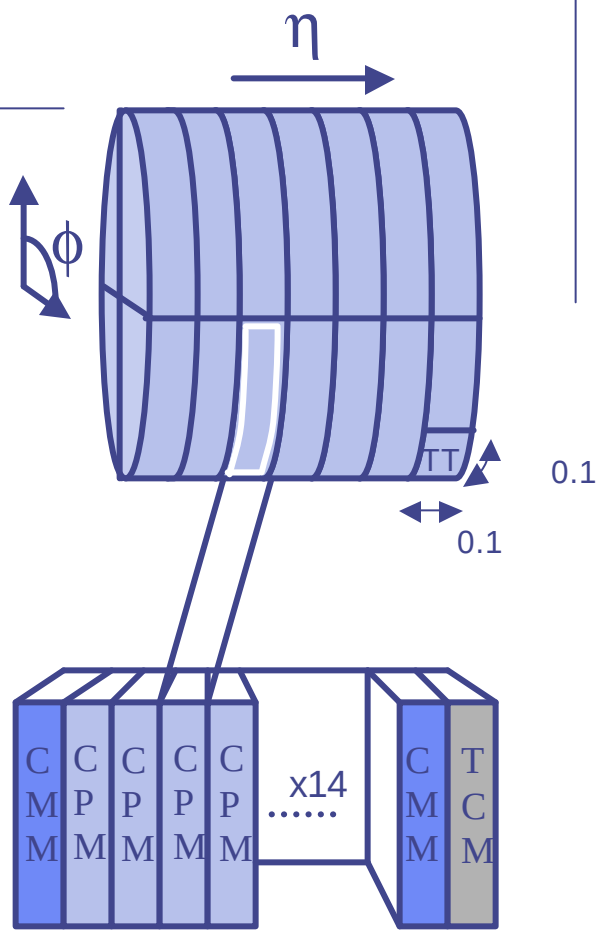


ATLAS Level-1 Calorimeter Trigger System



Cluster Processor Module (CPM): Requirements

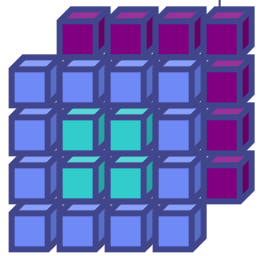
- Identify possible isolated electrons, photons and semi-hadronic τ decays for $|\eta|<2.5$
- Calculate multiplicities of e/γ candidates and τ/h candidates for different threshold conditions on E_T
- Transmit these multiplicities to Common Merger Modules (summing multiplicities from individuals CPMs) in real time
- Transmit Trigger Tower (TT) 0.1 x 0.1 (η x ϕ) data, multiplicities and RoI co-ordinates to ReadOut Driver (ROD) Modules at Level1A rate up to 100 kHz.



Cluster Processor Crate x4

Identifying cluster: Cluster Processor Chip

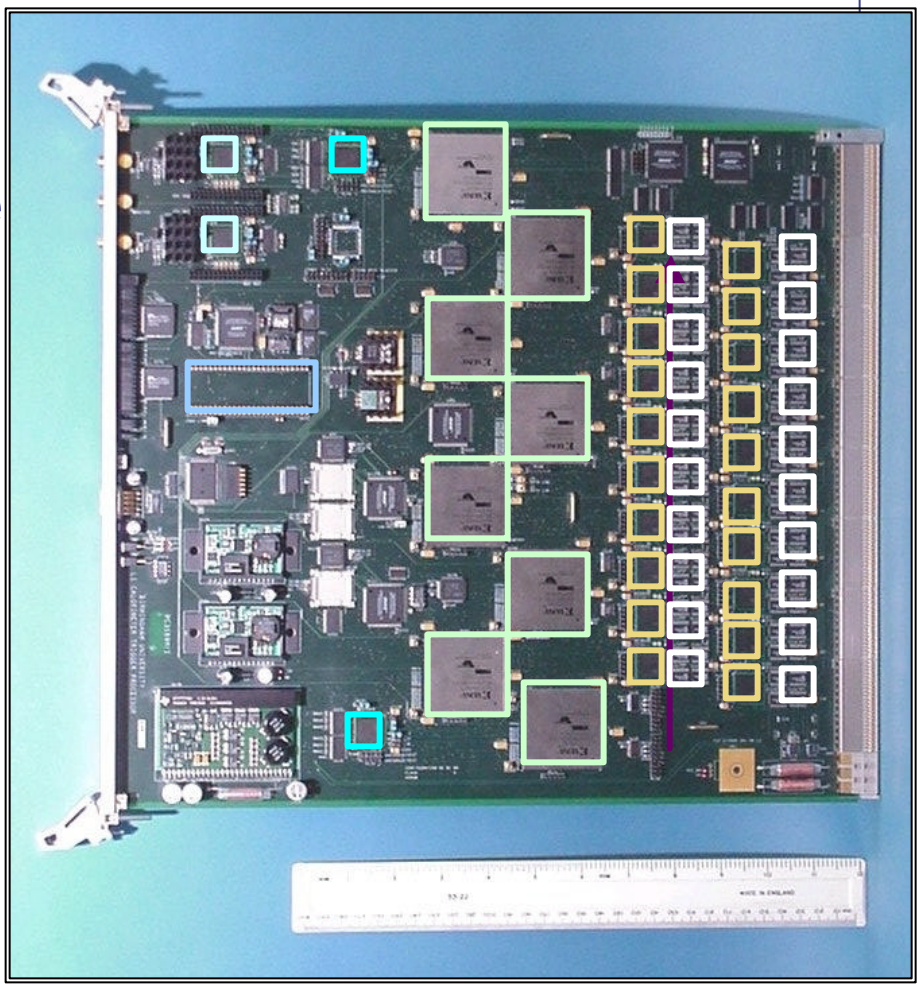
- A 4x4 window is defined for EM and Had: 32 TT in total
  - This window slides by 0.1 in eta and phi to fully cover the calorimeter
  - The RoI is defined by its (η,ϕ) coordinates and is a local maximum, if the window is a candidate trigger object
  - RoIs are tested against 16 sets of threshold values, each made up of cluster and isolation energies.



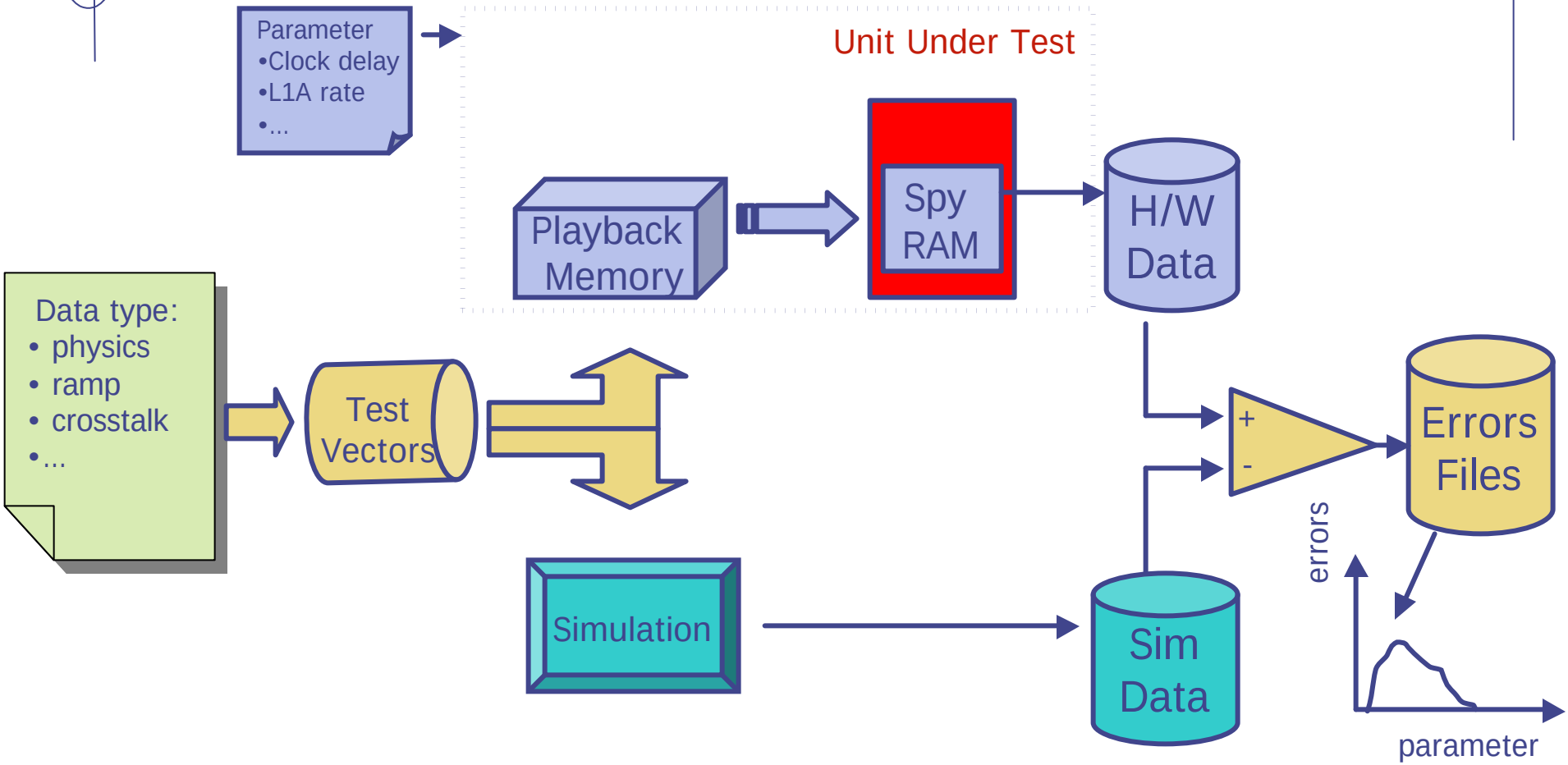
- Eight 4x4 windows are processed by one single FPGA chip XCV1000E
- 8 CP chips populate one CPM
- The limited available I/O requires serialisation of data @ 160 MHz
- Because the algorithm involves overlapping data, Trigger Tower data are shared:
  - between CP chips onboard
  - between CPMs, across a custom-built backplane

Cluster Processor Module: Implementation

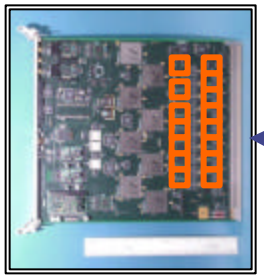
- 4 full specification boards have been made
- 80 LVDS deserialisers DS92LV1224
- 20 FPGA XCV100E Serialiser chips distribute data @ 160 MHz
- 8 FPGA XCV1000E CP chips perform the cluster finding algorithm
- 2 Virtex XCV100E merge multiplicities of all CP chips
- 2 Virtex XCV100E act as the readout controller of the RoIs and Data path
- 1 TTCdec card containing TTCrx chip to receive and decode TTC information from the backplane



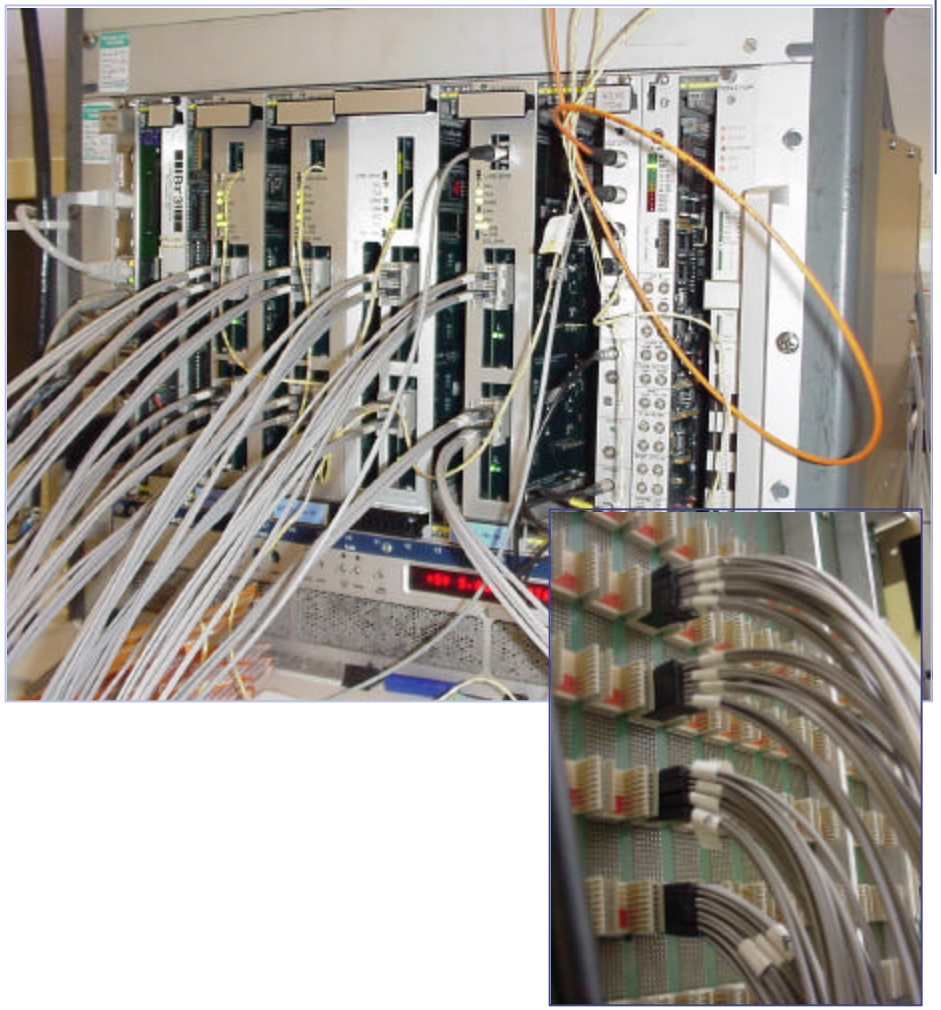
Cluster Processor Module: Testing Process



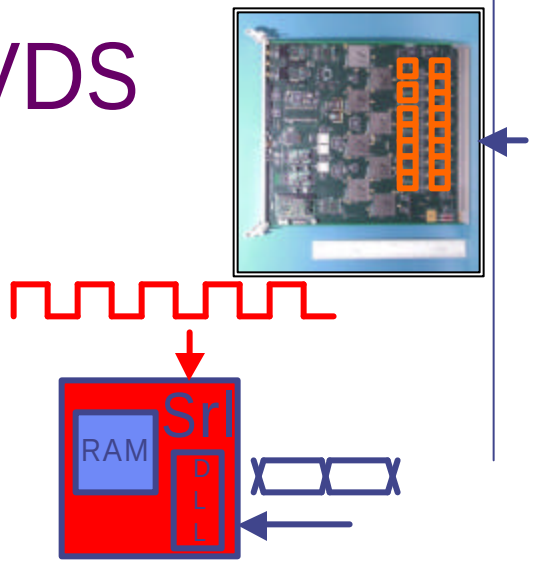
Cluster Processor Module: LVDS data input



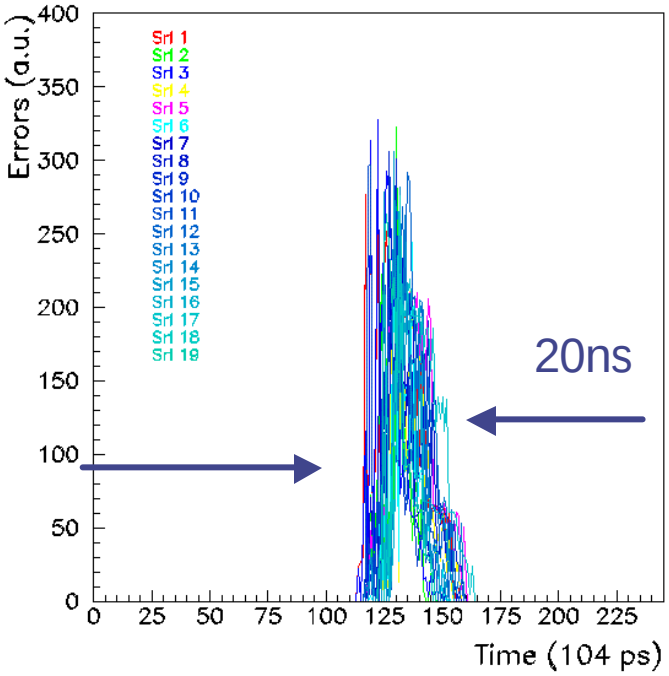
- Custom built Data Source Sink boards (DSS) have been used as source of 400 Mbit/s serial LVDS
- Five DSSs source a complete CPM
- A custom backplane receives the LVDS data from the rear (modules can thus be removed without uncabling)



Cluster Processor Module: LVDS Data Results

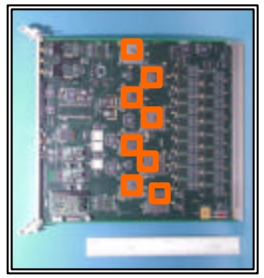


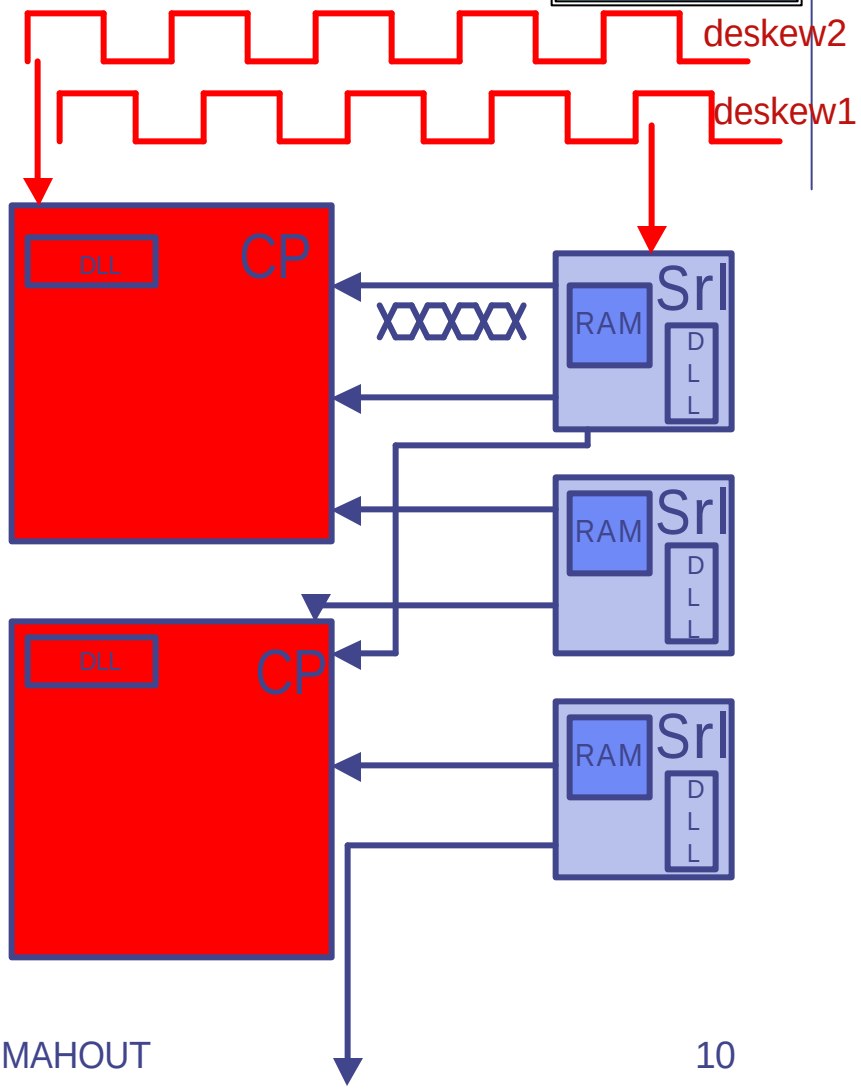
- Data at the input of the serialisers are strobed at 40 MHz
- TTCvi/TTCvx system was used to send the clock
- The serialiser chip clock was changed via the I^2C port of TTCrx
- Timing window measured by delaying input serialiser chip clock in 104 ps steps
  - Error free zone of 20 ns
- Bit Error Rate Test performed at the input of the serialiser chip: < 10^{-13} per channel with pseudo random data



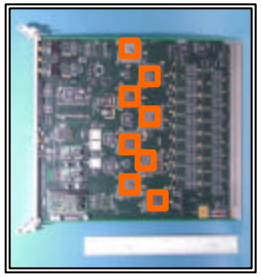
Cluster Processor Module: On board Real Time Data

- Serialiser playback memories were used to drive data to the CP chips
- Delay between CP chip clock (deskew2) and SRL chip clock (deskew1) was varied
- Delay was added using the available 104 ps step sizes

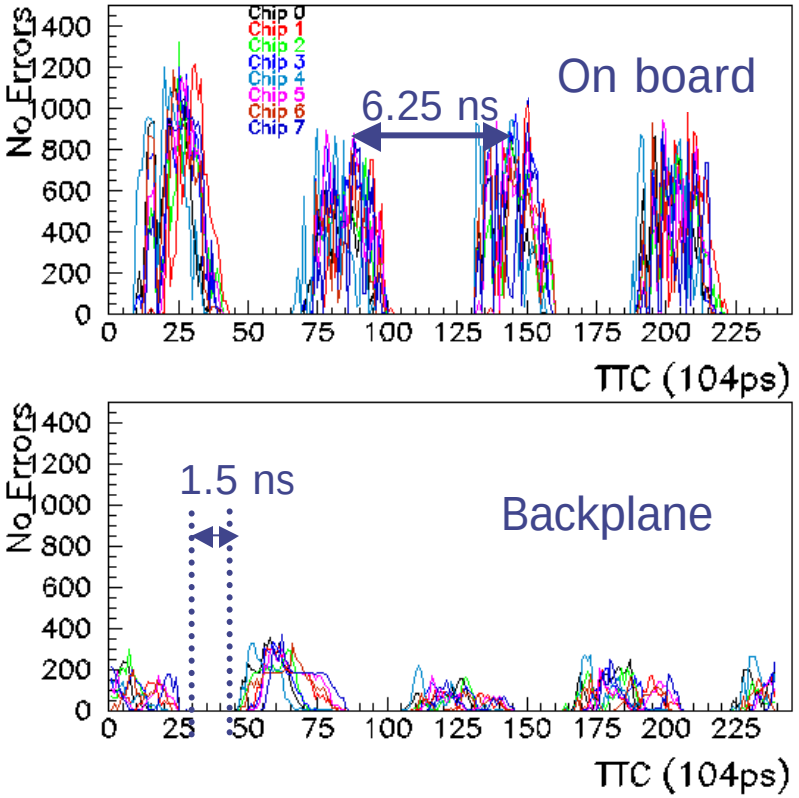




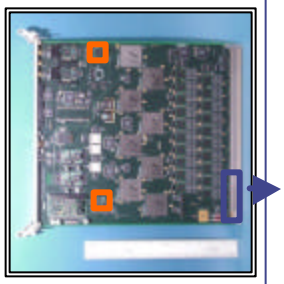
Cluster Processor Module: Onboard Real Time Data Test



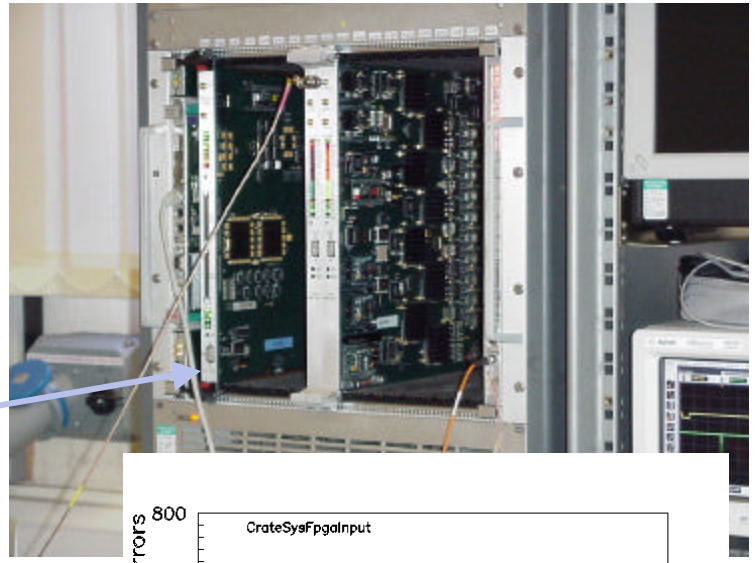
- 160 MHz data were correctly received inside the CP chips
- Error free timing window not bigger than 1.5 ns:
  - Length of tracks not optimized to minimize delay between lines
  - On-board Timing window per chip better than 2 ns
- Two delayed clocks are needed to match correct backplane data with on board data

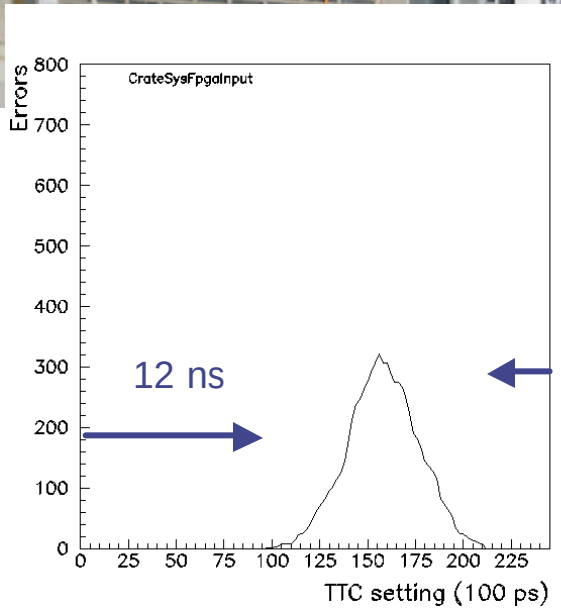


Cluster Processor Module: Hit multiplicities output

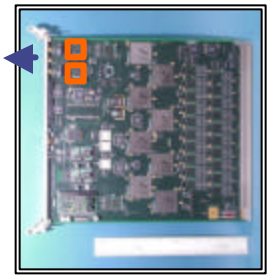


- Multiplicities of different thresholds are calculated in real time at the output of the Hit Merger chip
- Multiplicities are transmitted via the backplane to the CMM
- Hit data were recovered inside the spy memory of the CMM
- Timing scan was performed by delaying serialiser chip clock
- Error free timing window of 12 ns, the rest of the period spent to calculate the multiplicities





Cluster Processor Module: Readout Frame Definition

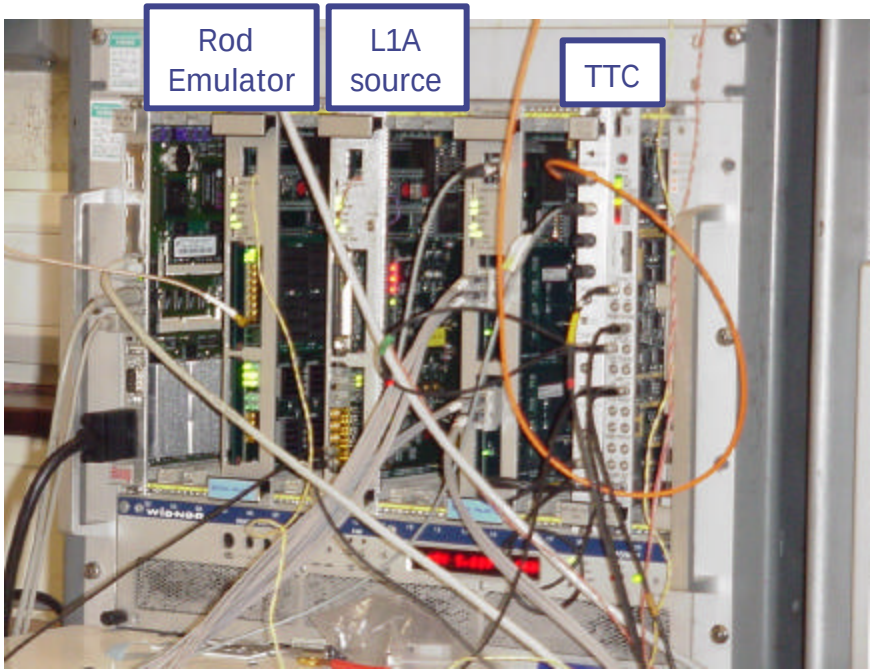


- RoIs found by the CP are stored in a FIFO and sent to a ROD with a Bunch Crossing Number (BCN) attached on each L1A

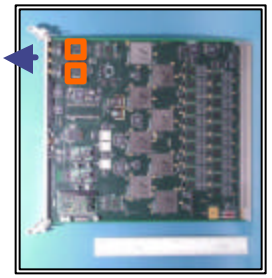
- DAQ monitoring data, consisting of energies from 80 TT as well as resulting hit multiplicities are also sent to a ROD on each L1A. Data from up to 5 consecutive bunch crossings can be sent

Cluster Processor Module: Readout Testing Setup

- DSS used as a source of L1A pulses with a known pattern
  - Nº and rate of L1A controlled
- TTCvi/TTCvx system used with external input signals
- Simulation data were generated according to known occurrence of L1As
- Error checks were performed on spy memory inside a ROD emulator (Glink Rx), on BCN and Data value



Cluster Processor Module: Readout Testing Results



- Burst rates of L1A up to 130 kHz were tested for Slice DAQ and RoI with no errors
- DAQ frame with the minimal required separation of 5 ticks between L1As were recovered successfully
- Up to 5 consecutive BCs DAQ data per event were also transmitted error free

Cluster Processor Module: Conclusions

- The CPM is a successful design
- Updated PCB layout for the final version needs only a few modifications:
  - Additional clock inputs per CP chip
  - Length of tracks optimized to reduce the timing spread
- These tested modules are to be used in integration test
- Updated design will be available for combined test beam next year