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ATLAS Level-1 Calorimeter Trigger and Central Trigger Processor

Overview

Signal Processing

Trigger Algorithms

Demonstrator

Future

ATLAS Level-1 Calorimeter Trigger

University of Birmingham, UK

University of Heidelberg, Germany

University of Mainz, Germany

Queen Mary & Westfield College, University of London, UK

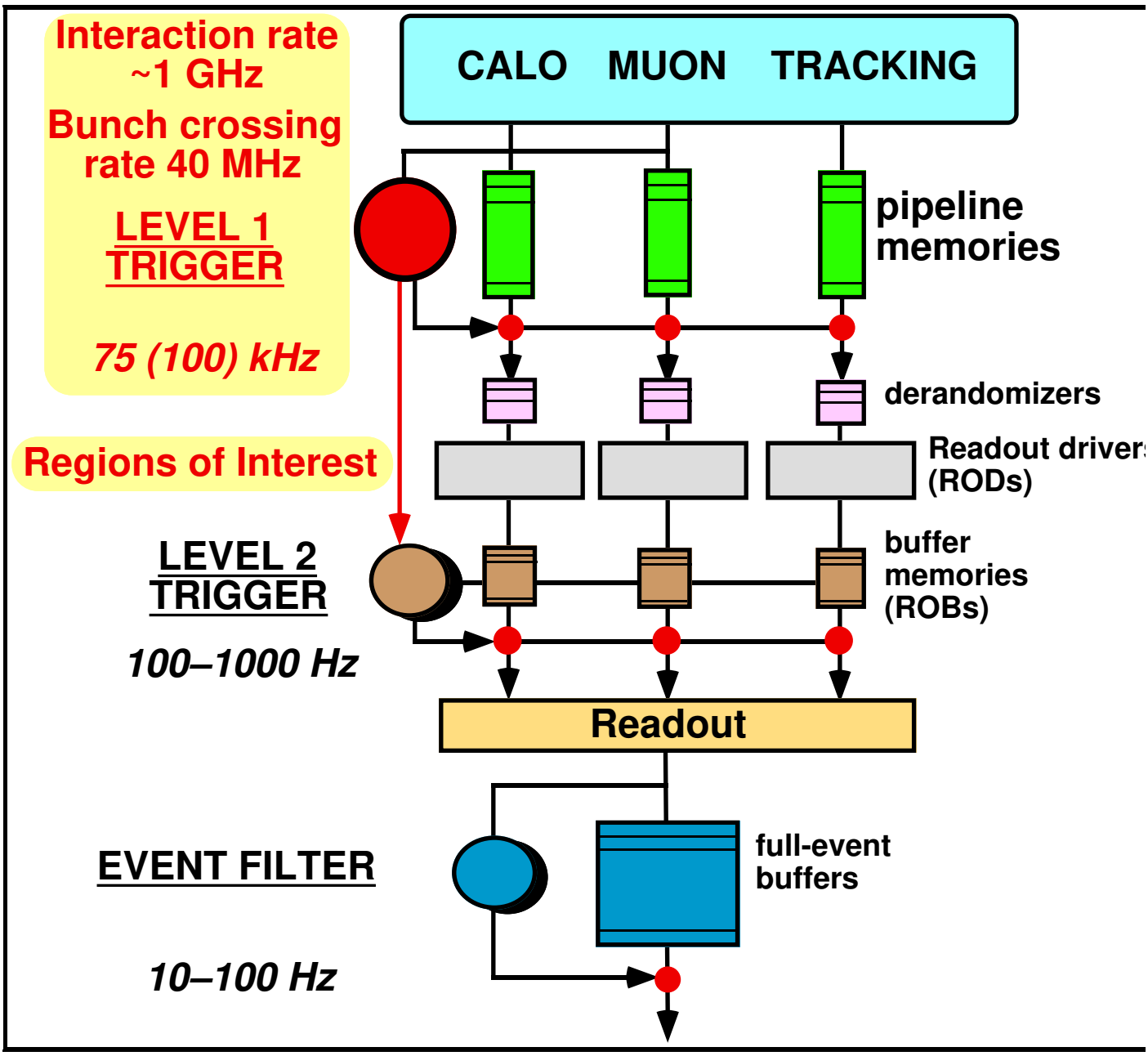
Rutherford Appleton Laboratory, UK

University of Stockholm, Sweden

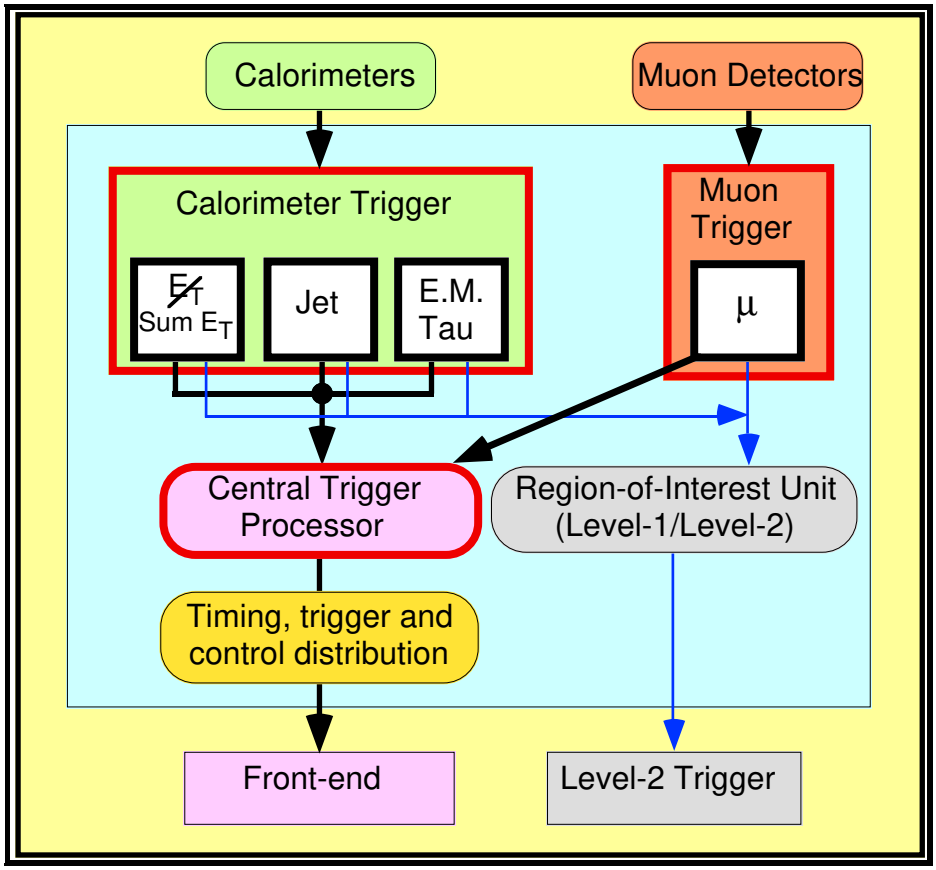
ATLAS Level-1 Central Trigger Processor

CERN

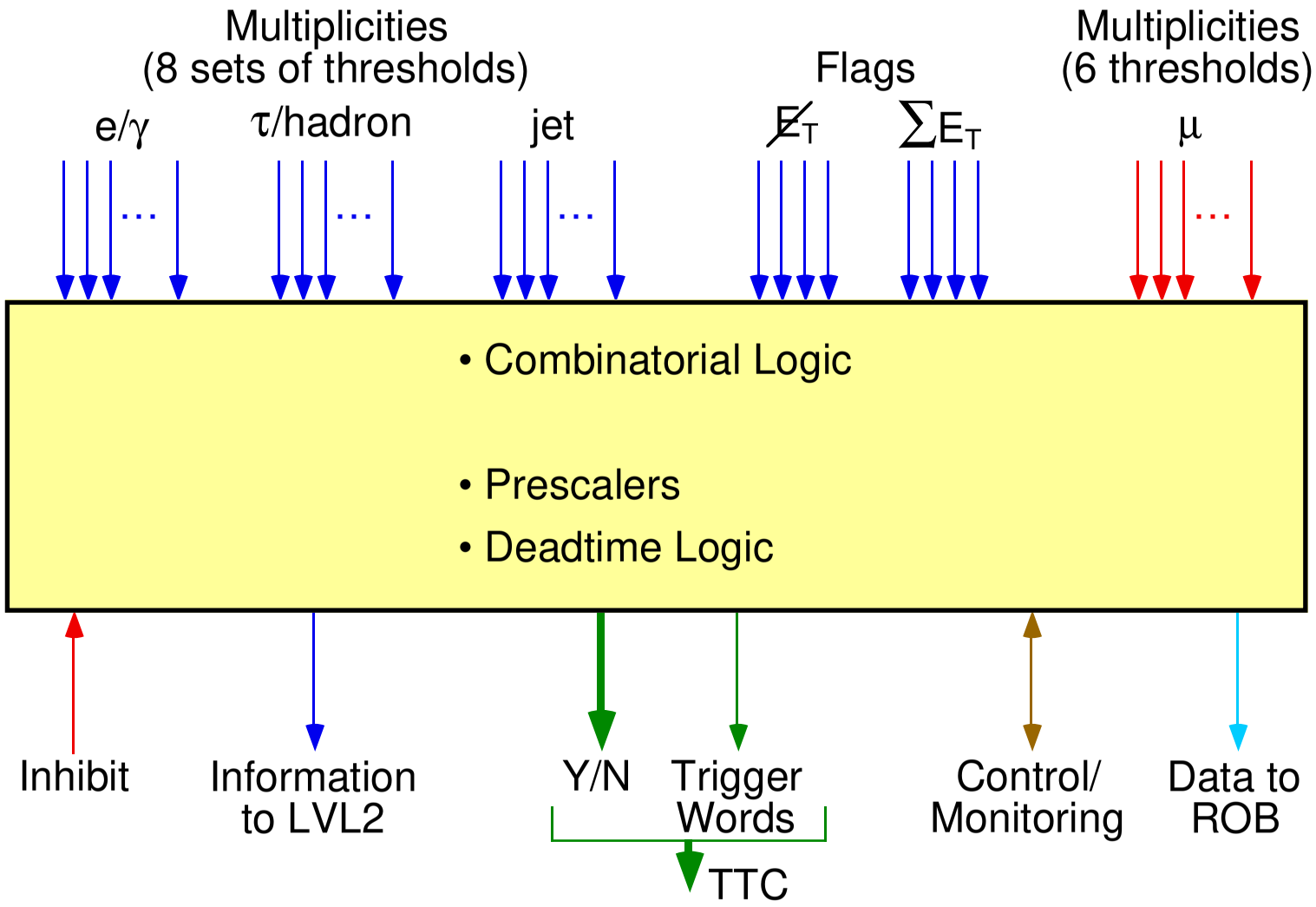
ATLAS Trigger System



ATLAS Level-1 Trigger



Level-1 Central Trigger Processor (CTP)



Final System: 96 combinations of 128 inputs

Demo System: 32 combinations of 32 inputs

Front-End Signal Processing

Raw Signals

- Summation by detectors into Trigger Towers, 0.1×0.1 in eta–phi.
- Analogue signals to trigger barrack by $\leq$80 m cable.
- Approximately 64×64 matrix of signals from both electromagnetic and hadronic calorimeters.

Signal Time Profile

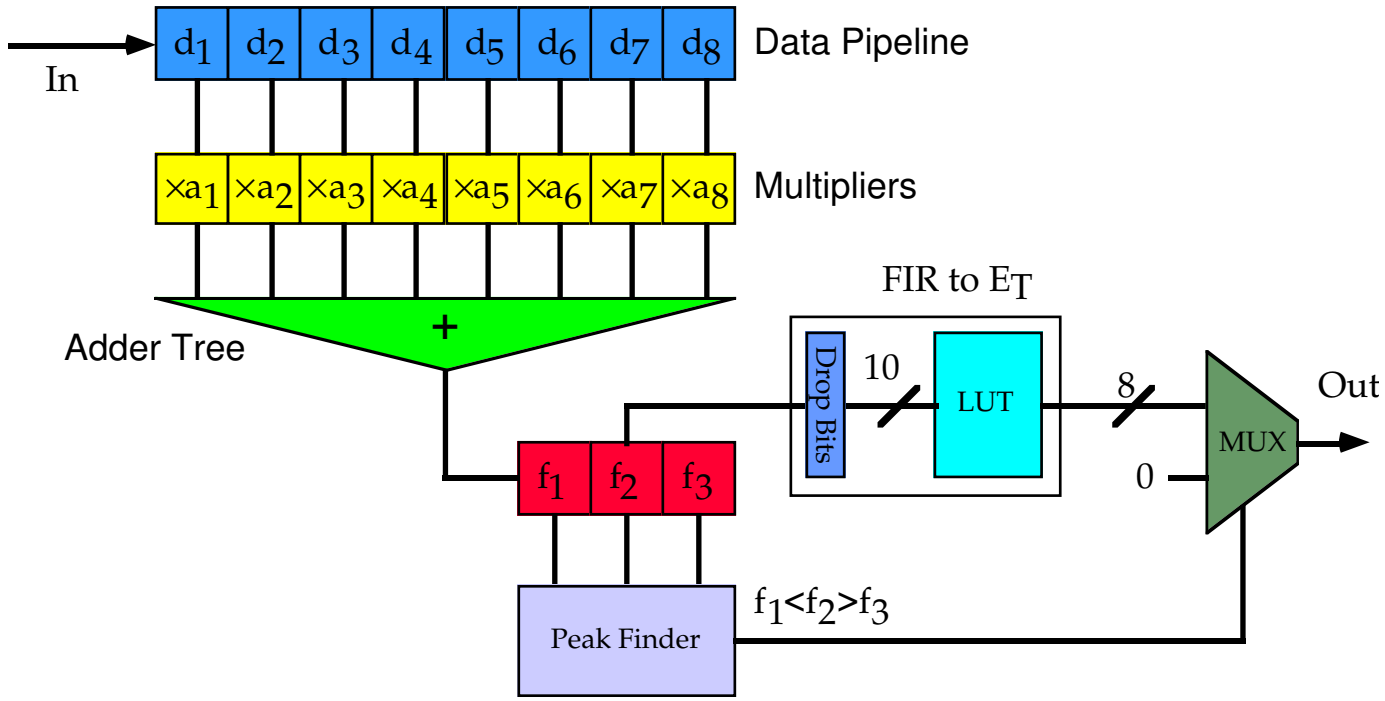
- Typical calorimeter signals last many bunch crossings.
- Different calorimeters have distinct time profiles.

Solution — Bunch-Crossing Identification (BCID)

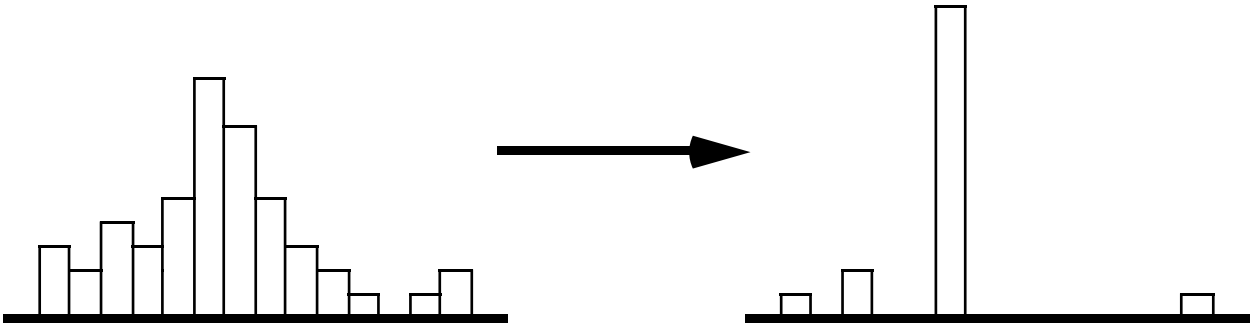
- Digitisation followed by programmable digital filter.
- Filter plus peak-finder extracts correct bunch crossing and transverse energy.
- Zero-suppression, calibration achieved in look-up table.

BCID Implementation

Circuit Schematic



Input and Output

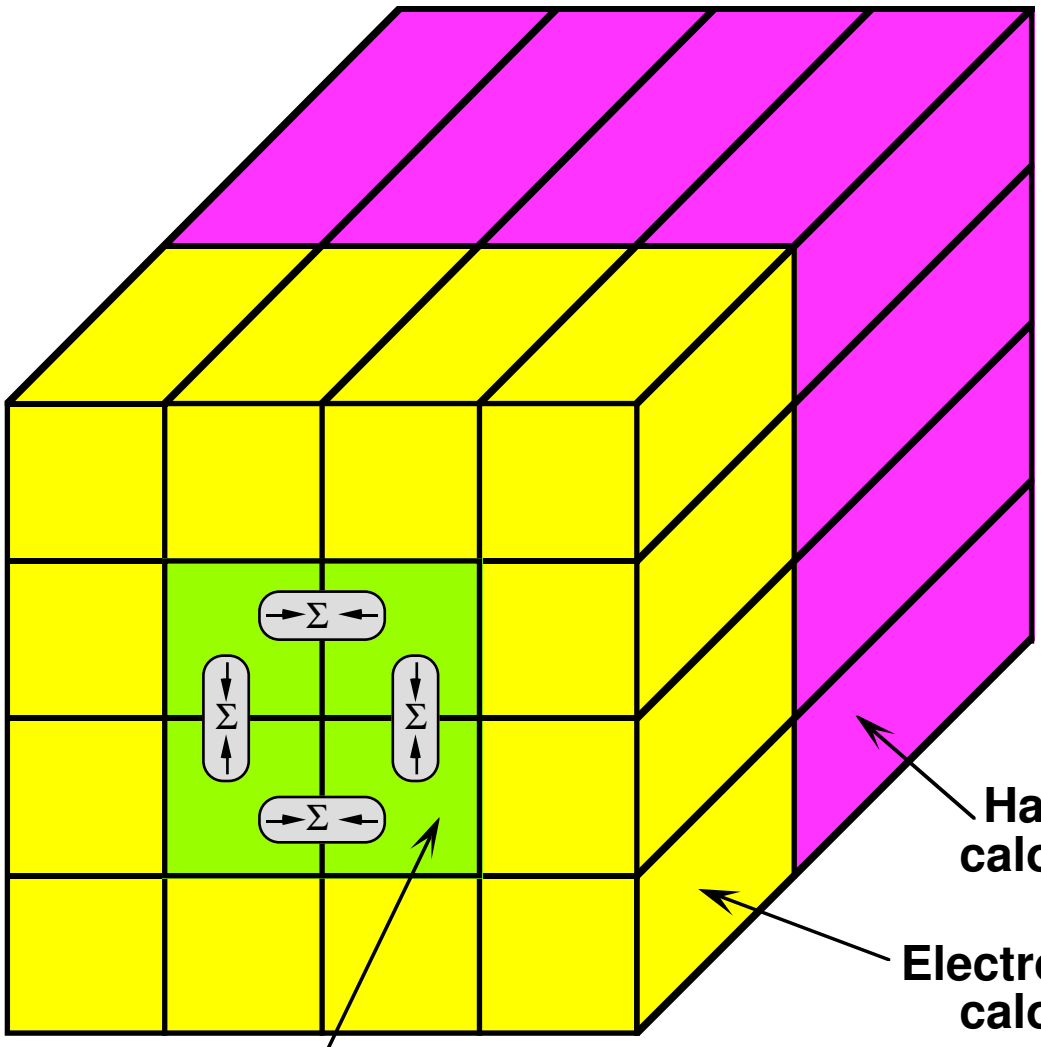


Calorimeter Triggers

- **Electron/photon – most difficult *(fanout)*, but algorithm well established.**
- **Jets – final algorithm still under review.**
- **Missing E_T – relatively simple.**
- **τ/hadron – similar topology to electron/photon.**
- **$\sum E_T$ – simple extension of missing E_T.**

Calorimeter E.M. Trigger Algorithm

- Most challenging part of trigger — must reject the overwhelming QCD jet background.



Σ Vertical Sums

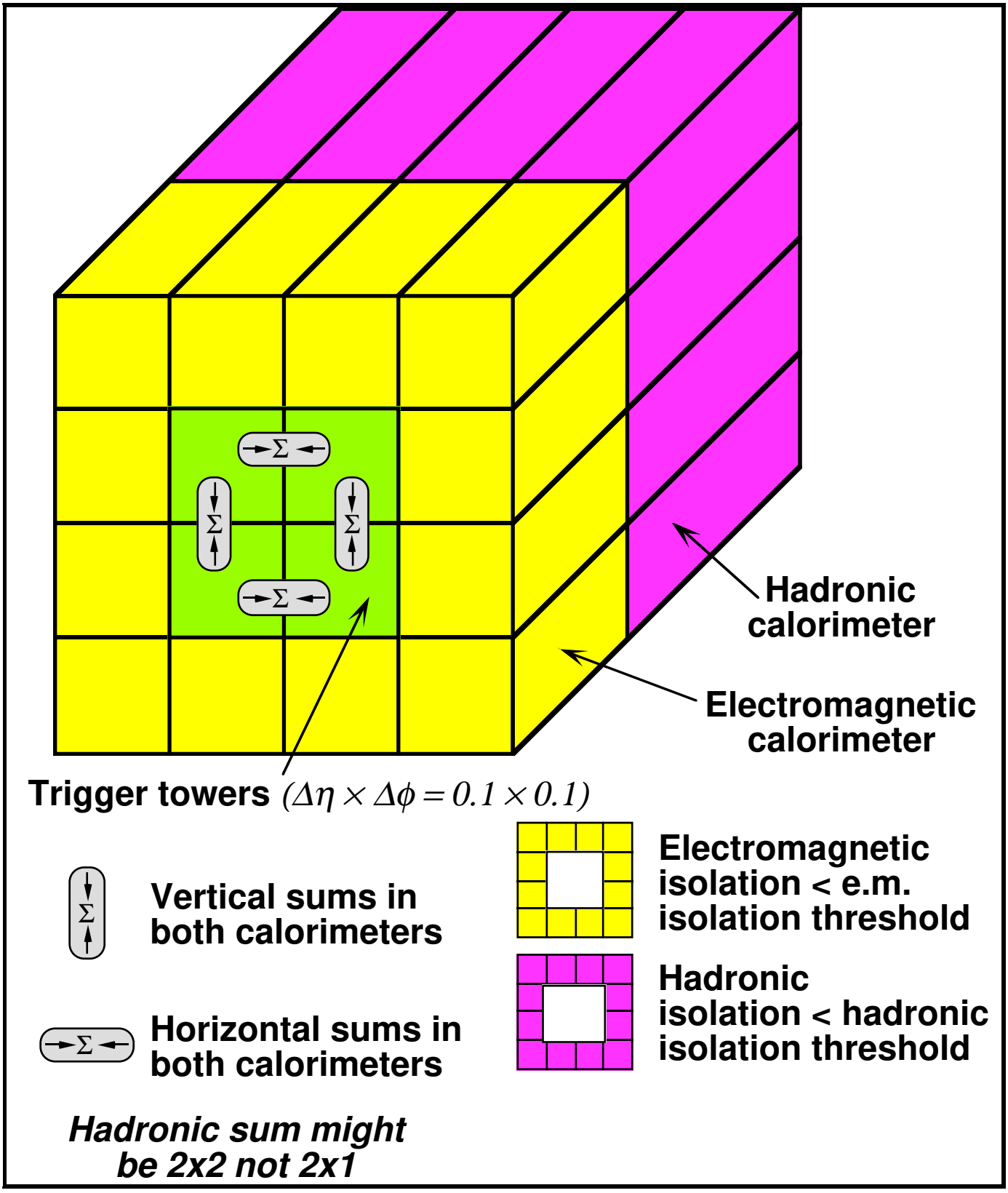
Σ Horizontal Sums

Electromagnetic isolation < e.m. isolation threshold

Hadronic isolation < hadronic isolation threshold

- ≥1 vertical or horizontal sum > cluster threshold E_T.
- Window slides by 0.1 in η and ϕ, so each trigger tower participates in 16 copies of the algorithm ⇒ massive fanout needed.

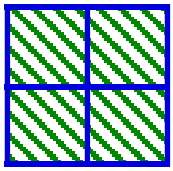
Single-Hadron (τ) Algorithm

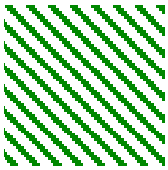


- ≥1 vertical or horizontal sum > cluster threshold E_T.

Jet Algorithms

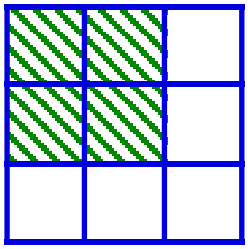
Window 0.4 x 0.4
Jet element/Slide 0.2 x 0.2
De-cluster/RoI 0.4 x 0.4, overlapping





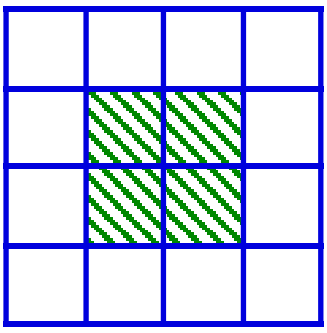
Note: De-cluster/RoI region is defined to be a local maximum in E_T

Window 0.6 x 0.6
Jet element/Slide 0.2 x 0.2
De-cluster/RoI 0.4 x 0.4, overlapping



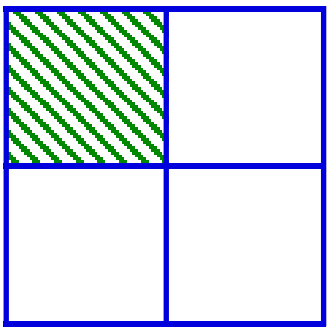
De-cluster/RoI can be in 4 possible positions

Window 0.8 x 0.8
Jet element/Slide 0.2 x 0.2
De-cluster/RoI 0.4 x 0.4, overlapping



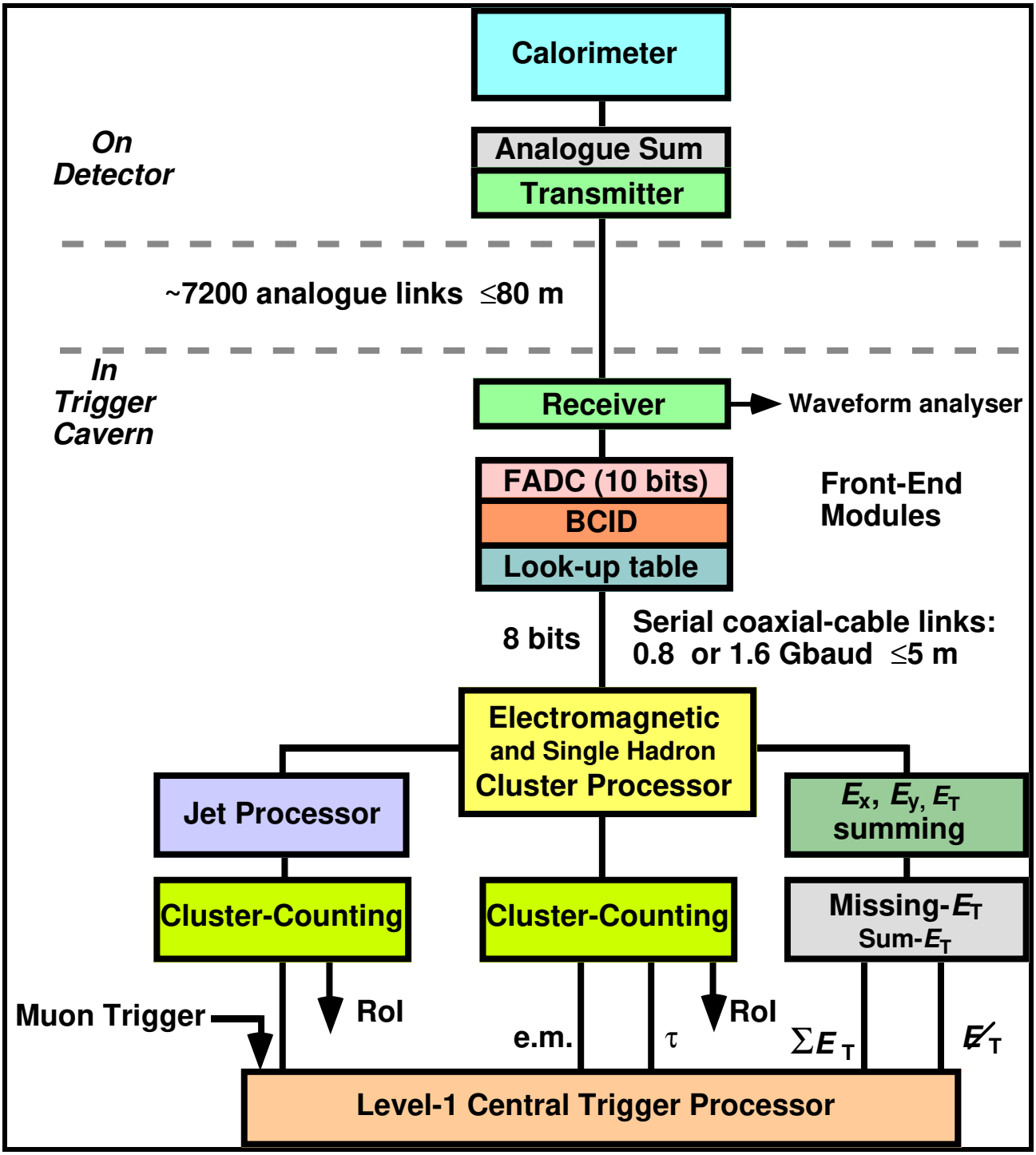
De-cluster/RoI must be in centre position (to avoid 5x5, and 2 jets/window)

Window 0.8 x 0.8
Jet element/Slide 0.4 x 0.4
De-cluster/RoI 0.4 x 0.4, non-overlapping



De-cluster/RoI can be in 4 possible positions

Calorimeter Trigger Structure



Research & Development

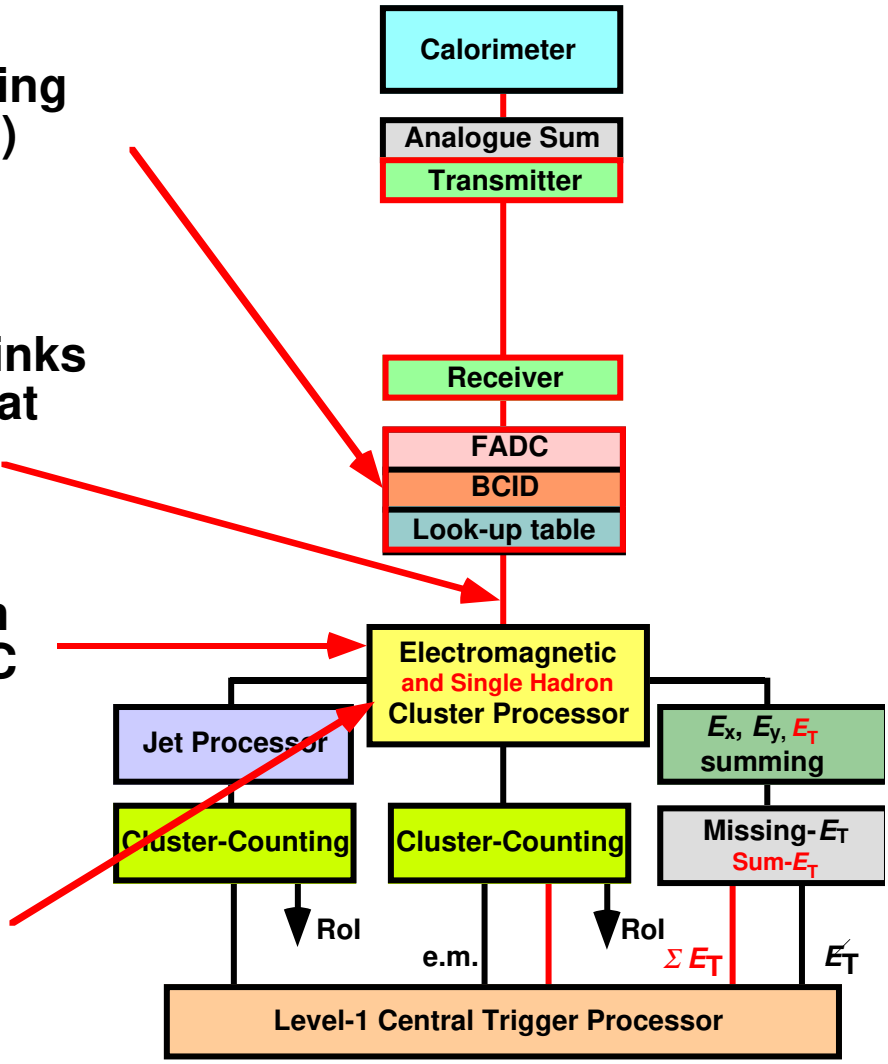
- **Beam Tests have been carried out in 1993, 1994, 1995, 1996 and October 1997, with both LAr and TileCal. Some highlights of past years ...**

1995
Efficient bunch-crossing identification (BCID) at 40 MHz

1996
Electrical (& optical) links run at 800 & tested at 1600 Mbaud

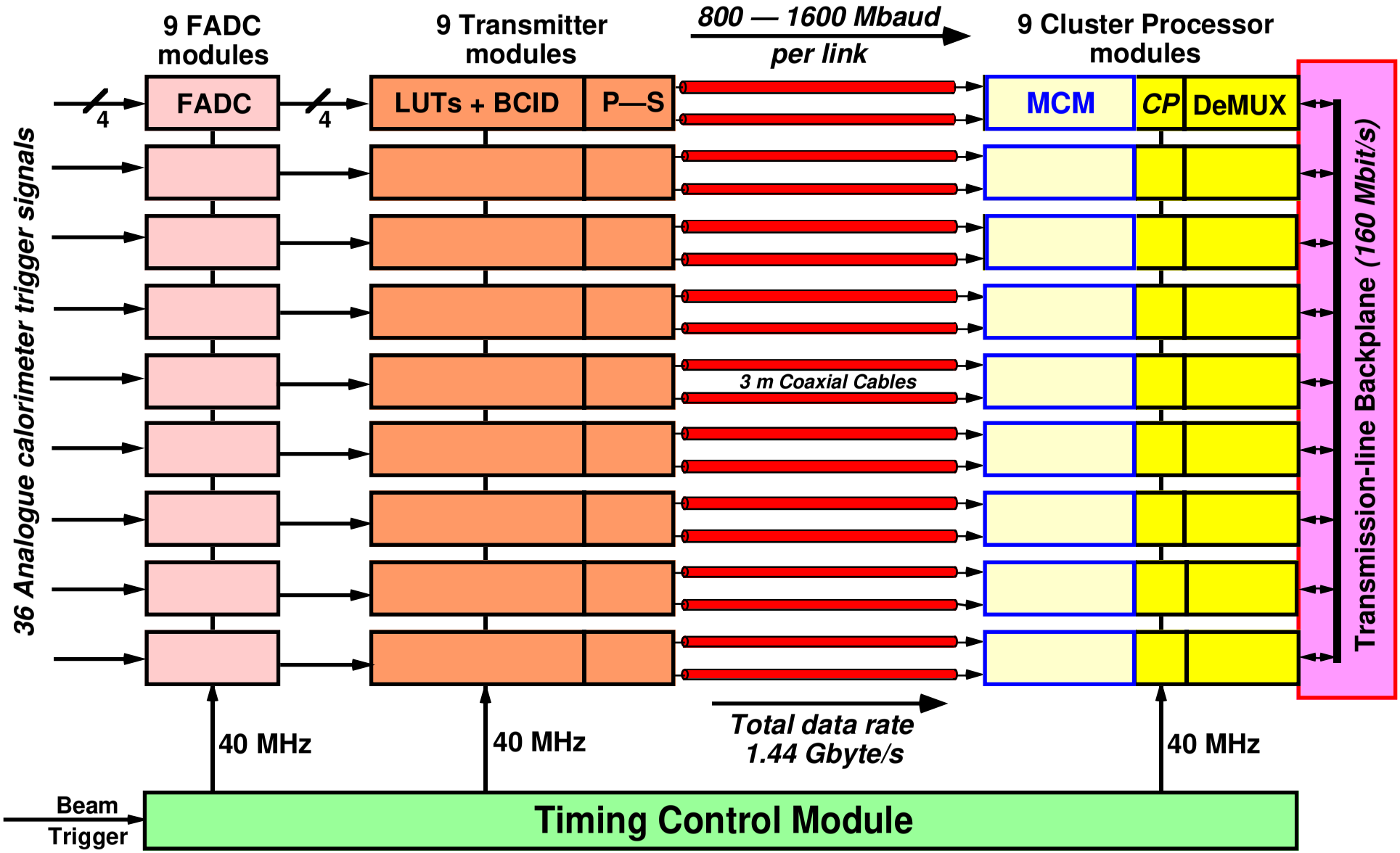
1994
E.M. cluster-finding in pipelined 40 MHz ASIC

1996
Multiplexing ASIC sending & receiving data at 160 Mbit/s

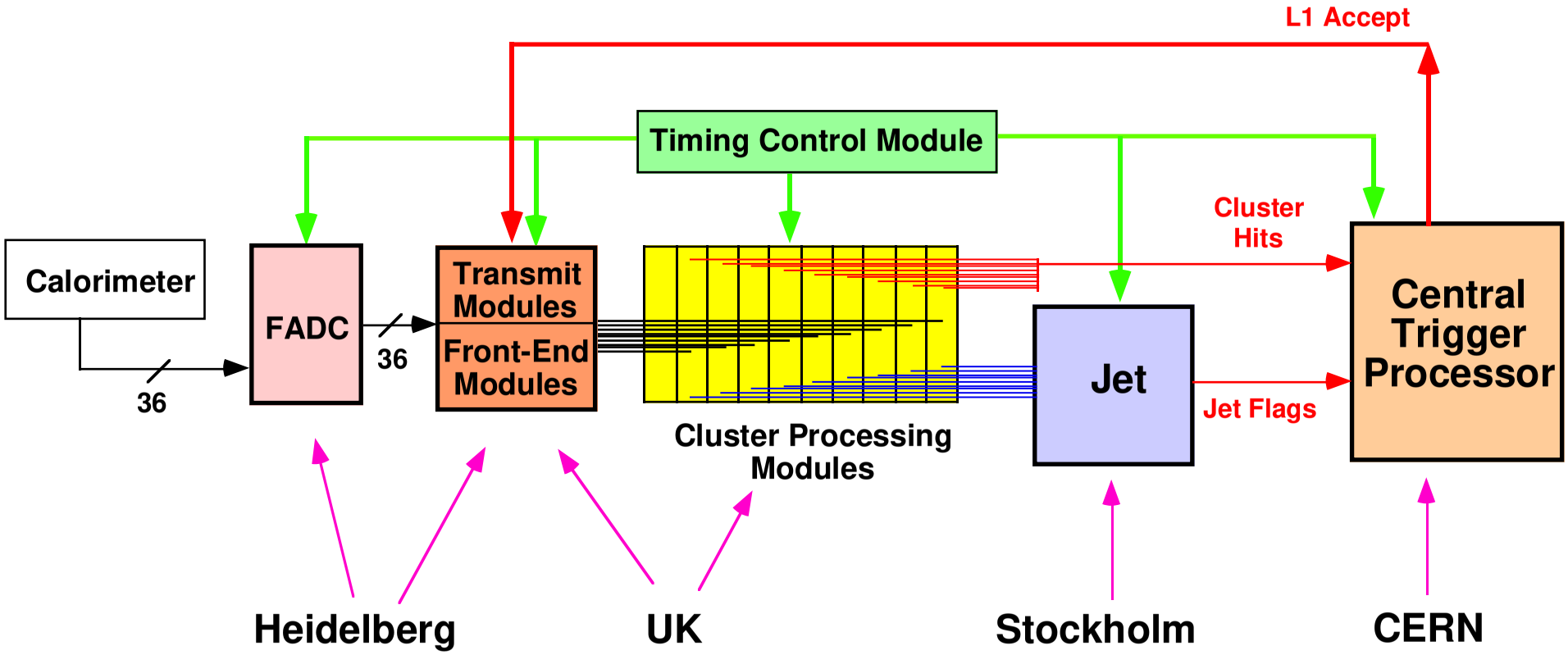


1996
Work was ended on the alternative proposal.
All groups are now working on a common design.

Data-Transfer Demonstrator 1997



Complete Slice Test 1997



Fast serial transmission using G-links

Why?

- **Needed to minimise input *(front-panel)* pin count on e.m. cluster processor modules.**

Technical points

- **800 Mbaud (640 Mbits/s data) ⇒ 2 channels/link.**
  This is minimum possible in current design.

- **1600 Mbaud (1280 Mbit/s data) ⇒ 4 channels/link.**
  Big savings on connections, chips, money, power…
  (32 vs. 64 G-link chips/module in final design)

- **Short links (< 5 m) ⇒ coax rather than optical fibre.**

Present status

- **800 Mbaud works very well. Bit error rate extremely low (~10^{-14}), link dropouts very rare.**

- **1600 Mbaud working. Bit error rate low. Some links suffer from occasional dropouts when there is nearby VME activity — probably due to noise, being investigated.**

Single-ended transmission on prototype backplane at 160 Mbit/s

Why?

- **Needed to minimise I/O pin count for channel fanout on e.m. cluster processor modules.**
  (384 signal pins per backplane connector in final design.)

Technical points

- **160 Mbits/s single-ended $\Rightarrow$ 2 lines/channel.**
- **3U prototype for 9-module demonstrator system.**
- **Data are transmitted as 100K ECL.**
- **Total backplane traffic in demonstrator system $\leq$ 35 Gbit/s.**

Present status

- **Tests using ECL look very promising: low error rates achieved with little tuning of timing or threshold levels. Apparent problems mostly traced to other causes.**

Multi-chip Modules

Why?

- **Needed for compact system, especially to minimise module count *(hence interconnections)* for fanout in e.m. cluster processing.**

Technical points

- **Prototype is first MCM designed at RAL.**
- **Includes 2 G-link and 2 160 Mbit/s MUX ASIC dies.**
- **Thermal management essential: ~6W.**

Present status

- **Prototypes currently being tested.**

Future Plans for Calorimeter Trigger

- **Discussion of trigger algorithms and performance**
  Next week

- **Jet algorithm decision**
  December 1997

- **Final laboratory tests to verify data transport integrity**
  → January 1998

- **Architecture design**
  February–March 1998

- **ATLAS internal review**
  March 1998

- **TDR**
  June 1998