Study of LVDS Serial Links for the ATLAS Level-1 Calorimeter Trigger

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Abstract

This paper presents an evaluation of the proposed LVDS serial data transmission scheme for the ATLAS level-1 calorimeter trigger. Approximately 7000 high-bandwidth links are required to carry data into the level-1 algorithmic processors from the Preprocessor crates. National Semiconductor's Bus LVDS serialiser/deserialiser chipsets offer low power consumption at low cost and synchronous data transmission with minimal latency. Test systems have been built to measure real-time bit-error rates using pseudo-random binary sequences. Results show that acceptable error rates better than 10^{-13} per link can be achieved through compact cable connector assemblies over distances up to 20 m.

I. Introduction

The ATLAS level-1 calorimeter trigger [1] requires approximately 7000 high-bandwidth serial links to transfer data from the Preprocessor into the algorithmic processor systems. Each processor module must receive data in excess of 4 GByte/s over these links, with minimal latency and a bit-error rate (BER) better than 10^{-10} for each link.

Serial data transmission has been chosen because the large data volume (about 800 bits/event per module) makes parallel transmission unfeasible. The serial links must be able to accept and transmit data arriving at 40 MHz, which is the LHC bunch-crossing (b.c.) rate. The trigger data fit most efficiently in 20-bit words, so a serial link chipset with either 10 or 20-bit frame width is preferred to avoid wasted bandwidth.

II. Requirements on serial link chipsets and cables

A. Requirements on serial link chipsets

It was originally proposed to use Agilent (HP) HDMP-1022/1024 G-link chipsets [2], which have performed well in tests, but their very high power consumption gave cause for concern over crate power and cooling issues. LVDS links offer much lower power consumption, and the National Bus LVDS serialiser/deserialiser DS92LV1021/LV1212 and LV1023/1224 chipsets [3] are easily interfaced to the trigger system while transmitting data synchronously with minimal latency. An overview of advantages and disadvantages of the two chipsets is shown in Table 1. The Agilent HDMP-1032/1034 chipset is ruled out because of its 16-bit frame size, though it has improved power consumption. The transmitting chip will be situated inside a Multi-Chip Module, therefore it must be available in die form. The package size must also be compact, since the receiving modules are populated with up to 96 link receivers.

B. Requirements on cable assemblies

The processor modules will share data via a high-speed backplane, and the LVDS links will be connected through this backplane rather then the front-panel in order to allow easy installation and replacement of modules. Compact cable assemblies are needed because of the high channel count per module: up to 96 LVDS channels per module are required and each 9U processor module requires up to 830 backplane pins. A Compact PCI-type connector series has been chosen to match those requirements, therefore cable assemblies need to have matching connectors. The tests focused on the following cable types, which are all halogen-free:

Table 1
Comparison of serial link chipsets. Advantages are shown in **bold**.

	Agilent (HP) HDMP-1022/1024	**National Sem. DS92LV1201/1212**
Frame Size at 40 MHz	20/21 bits (800 Mbit/s)	10 bits (400 Mbits/s)
Device Power Consumption	2.5 W	**0.15 W**
Supply Voltage	5 V	**3.3 V**
Total Power per Module	100 W	**12 W**
Cost/Tower (May 2000)	≈ $170 Tx+Rx	≈ **$30** Tx+Rx (x2 for 20 bits)
Specified Frame Rate	7.5–75 MHz	16–40 MHz
Connection Methods	DC, AC, Optical Single or diff.	DC diff.

- Kerpen Megaline 726 flex AWG 26 ethernet patch cable [4]
- Detwyler Uninet flex 4P 600 MHz ethernet cable [5]
- AMP 1370754-1 AWG28 cable assembly with 2 mm Z-pack connectors. [6]

Both the Kerpen and Detwyler cables contain four individually-shielded twisted pairs, are relatively stiff, and are fitted with bulky connectors. The AMP assembly contains four individually-shielded parallel pairs, is more flexible, and is fitted with compact 2 mm connectors matching the connectors chosen for the system backplane.

The final installation within ATLAS requires inter-crate links over distances of 10–15 m, and a low bit-error rate is crucial for these links in order to minimise false triggers. In order to have a significant safety margin, the tests were run using cable lengths of up to 20 m.

For minimum latency, only error detection, not correction, is possible. To minimise the error rates, the cable assemblies being considered require some form of equalisation for the attenuation at high frequencies, as the raw data rate on each link is 480 MBaud. Both active and passive pre-compensation techniques at the transmitter have been investigated.

III. LVDS Link Test Setups

Three separate test systems were produced at Birmingham, Heidelberg and Mainz. These involved up to eight channels in parallel, and measured bit-error rates for differing combinations of precompensation, cable length and cable type. Test systems were designed to transmit and check pseudo-random and repetitive data patterns in real time in order to achieve the statistics required for measurements of very low bit-error rates.

In order to do full speed tests with high statistics, the data patterns transmitted via the serial link have to be checked for bit errors on-board, which is done using programmable logic devices (FPGAs) on the test modules. Error counters are implemented for long-time link stability tests: one per link channel counts every mismatch of the expected bit pattern and the data word actually received, and a second one counts all link breaks, which can be detected by a rise of the LOCK pin on the LVDS deserialiser.

A. LVDS Link Tests with TTC clock at Birmingham

The LVDS Link evaluation setup at Birmingham (see Figure 1) used *Data Source and Sink (DSS)* VME modules [7] fitted with LVDS Serialiser and Deserialiser Common Mezzanine Cards (CMC). The DSS+LVDS combination was clocked from a TTC test system, using the TTCrx ASIC [8]. Up to eight LVDS link channels have been tested running simultaneously. Xilinx FPGAs on the DSS modules were used to generate pseudo-random bit patterns and detect bit errors within the data words after transmission over the LVDS link. A passive precompensation circuit shown in Figure 2 is used to equalize for the cable impedance at long lengths greater than 10 m and high frequencies.

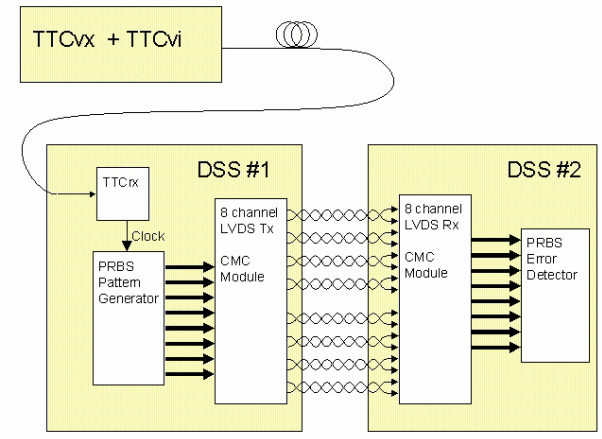

Figure 1: LVDS test setup using DSS motherboard, clocked from TTC system.

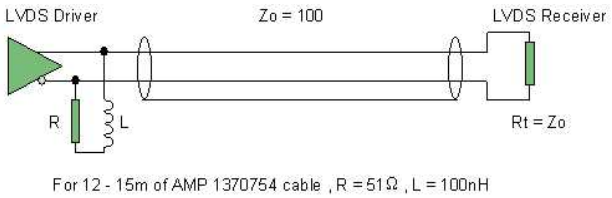

Figure 2: Precompensation method using LR (100mH, 51 Ω).

Initial results showed the original LVDS deserialiser DS92LV1210, when run at its maximum frequency of 40 MHz, had little tolerance to power-supply noise and clock jitter. Although most links could be run with error rates less than 10^{-13}, some showed errors at levels of about 10^{-12} even with significant power-supply filtering. These parts could only be used provided that:

- Transmitters were fed from a high-stability clock source,
- Receiver supplies were heavily filtered, and

- Cable HF loss was over-compensated.

A faster LVDS chip set has recently been released, and the LVDS link tests were repeated using the faster deserialiser part DS92LV1224. This device has an improved timing margin on incoming data compared with the original part, and showed much better tolerance to power supply noise. A comparison of those two chipsets is given in Table 2.

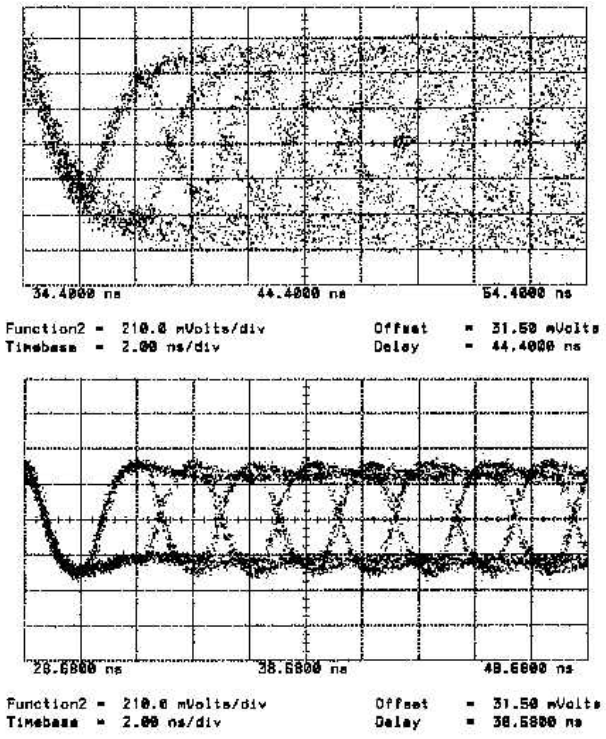

Figure 3: Stream of pseudo-random patterns after 15 m Detwyler ethernet cable at receiving end (LV1212). Top: no precompensation, bottom: with precompensation using LR.

Table 2
Comparison of serial-link chipsets when operated at 40 MHz.

Parameter	Original devices (LV1210/LV1212)	New devices (LV1212A/LV1224)
Timing Margin	100 ps	450 ps
Receiver Threshold (max)	100 mV	50 mV
Power Consumption	145 mW	191 mW
Latency	1.75 b.c.	1.75 b.c.

No errors were found after several overnight tests on various cable assemblies, including 15 m of high-density AMP cable and 20 m of Datwyler ethernet cable. A total of 3×10^{13} bits were sent without error over each link. These faster parts no longer need a high-stability 40 MHz clock source feeding the transmitter. The cable equalisation circuit is less critical, with circuit values now covering a much larger range of cable lengths.

B. LVDS Link Tests at Heidelberg

The LVDS link test setup at Heidelberg shown in Figure 4 used two VME motherboards of the *Modular VME Test System* (described in [9]) as carrier for two CMC daughter-boards. Two CMC cards were designed: a sender daughter-board carrying two LVDS serialisers (DS92LV1021) and a receiver daughter-board with two LVDS deserialisers (DS92LV1212). Cables by

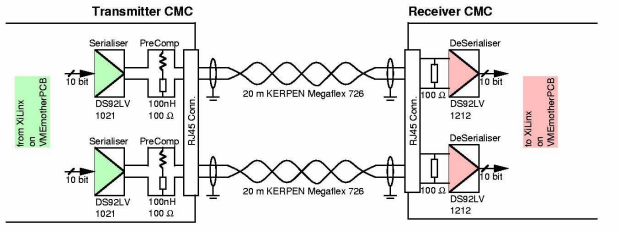

Figure 4: LVDS link test setup at Heidelberg.

Kerpen and AMP already described above were used for serial data transmission at lengths of both 15 m and 20 m.

Bit-error rate measurements are performed using a Xilinx FPGA and a dual-port memory sited on the motherboard, and which are programmable from a host computer via VME. Various patterns can be tested, either pseudo-random bit patterns, or repetitive patterns which might be critical for link stability.

Several sets of measurements were performed in order to test data integrity across the transmission assembly. Passive precompensation for the cable on the transmitting side of the data-link has been incorporated, using an inductance (10 nH) in series with a resistor (100 Ω) between the differential pair carrying the serial data stream. In Figure 5, a pseudo-random stream is shown at the transmitting and receiving end. A significant loss of average signal amplitude has been observed due to the additional resistor across the differential pair. However, the inductance led to a sharpening of the leading edges for each transition, compensating for the integrating effect of the cable itself.

The beneficial effect of the precompensation can be determined best by examination of the data stream at the receiving end after the cable, as shown in the bottom part of Figure 5. There is a loss of average amplitude with precompensation. But the cleaner and wider open eye-pattern for every data-bit is also clearly recognizable. The net result is safer operation of the data-link in terms of bit-error rates. The input sensitivity of the LVDS receiver is 100 mV in amplitude, which is only about one-half of the vertical opening of the bit eye-pattern. Reliability of data transmission is not only secured by sufficient amplitude, but also by sufficient width on the time-scale.

C. LVDS Link Tests at Mainz

The LVDS link test setup at Mainz, shown in Figure 6, included a modified version of the *Jet/Energy-sum Module*

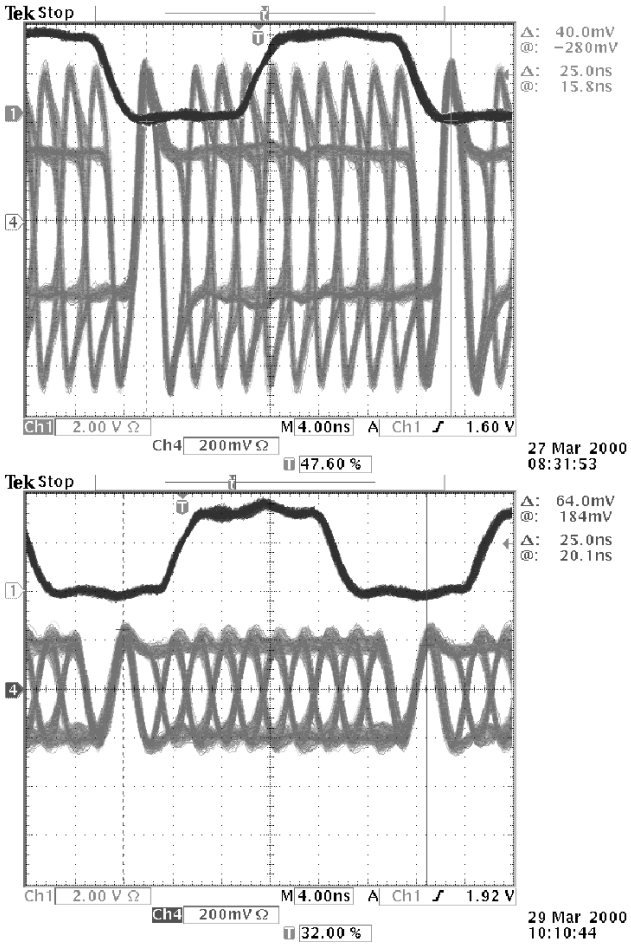

Figure 5: LVDS link signals: effect of cable length. Top: a transmitting end (LV1021), bottom: at receiving end (LV1212) after 20 m cable (AMP assembly with 2 mm connectors); also shown: 40 MHz crystal oscillator.

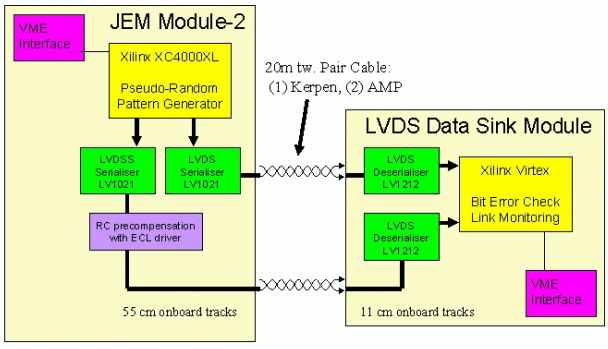

Figure 6: LVDS link test setup at Mainz.

technology demonstrator (JEM '–2') equipped with two LV1021 serialiser parts as LVDS link sources. A programmable logic device (Xilinx FPGA) on the board is used to provide clock strobes and generate the bit pattern. The JEM '–2' includes 55 cm of differential onboard tracks (Z=100 Ω). The *LVDS Data Sink Board* receives the data using two LV1212 deserialisers. A Xilinx Virtex FPGA does bit-error checks and monitors the stability of the link lock. The LVDS data sink board has 11 cm of on-board tracks (micro-striplines).

An active precompensation circuit has been added at the transmitting end, which is shown in Figure 7. An RC circuit and an ECL driver (EL 89) are used with reference voltage adapted to LVDS signal levels. Cables by Kerpen and AMP

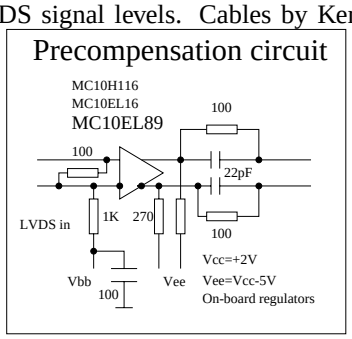

Figure 7: Active precompensation with RC using ECL driver.

already described were used for serial data transmission, at lengths of both 15 m and 20 m. The Data Source and the Data Sink modules were installed in two different VME crates, both constantly accessed from host computers via VME in order to test the system for stability against noise produced by such activity.

In order to generate a signal load similar to the final system on the module on both the serial and parallel side of the links, a circuit was built to supply all eight LVDS deserialisers, with one receiving valid data, and the other seven used as 'noise generators'. It was also found that the Xilinx Virtex FPGA series needs heavily-filtered power supplies (see [10]), otherwise the noise generated by those devices can cause bit errors on the LVDS link.

A bit error rate of 10^{-13} on one channel using 20 m of AMP cable was reached, which was limited only by the time of the test run. It was observed that long on-board tracklines cause attenuation of the LVDS signals similar to long cables. Without the precompensation circuit the maximum cable length without bit errors decreased significantly when using the on-board tracks for transmission. This effect, however, was not seen again when precompensation was used. It was concluded that the length of the tracklines from the cable connector to the link deserialiser should be minimized on future modules in order to optimize the signal quality at the receiving end, therefore improving link stability.

IV. Test Results

The National Bus LVDS serialiser/deserialiser chipsets (DS92LV1021/LV1212 and LV1023/LV1224) are easily interfaced to the trigger system while transmitting data synchronously with minimal latency. BERs better than 10^{-13} per link have been achieved with cable lengths from 10 m to 20 m even with simple and straightforward LR equalisation.

Experience with the first-generation chipset (LV1021/LV1212) showed that use of these parts was not straightforward, operating as they are at the limit of their

specified data rate. The causes of power supply noise must be kept to a minimum, and board layout is critical. In particular, it is important to ensure that the transmitter clock has a low level of jitter. However, the problems encountered have been understood and solutions found.

However, the later version of the deserializer (LV1224/LV1212A) device was found to be much less sensitive to clock jitter and needs less power supply decoupling. Therefore, those devices were chosen for the prototype modules. Also, this latest chipset has higher operating frequencies (40–66 MHz), which allows it to run at the lower end of its rate specification in the level-1 trigger system.

Regarding the choice of cables, it was found that the AMP assembly matches the requirements of the system best, both electrically and mechanically. It is flexible and is fitted with compact 2 mm connectors, which can be easily fitted to the backplane of the processor systems

V. Conclusion

In conclusion, the LVDS links form a viable scheme for transfer of large volumes of data, having the advantages of low latency, low power and low cost. They also offer high-density connectivity, which is essential for compact cable plant. Prototype processors are now being designed that will incorporate a large number of such links.

VI. References

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[3] National Semiconductor DS92LV1021/ LV1212/ LV1224 datasheet `http://www.national.com/appinfo/lvds`

[4] Kerpen Website: `http://www.kerpen.com`

[5] Detwyler Website: `http://www.datwyler.co.uk`

[6] AMP website: `http://www.amp.com`

[7] DSS Data Source and Sink Module - Specifications `http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html`

[8] RD12 - Timing, Trigger and Control (TTC) Systems for LHC Detectors at CERN: `http://ttc.web.cern.ch/TTC/intro.html`

[9] Volker Schatz, *Test of a Readout and Compression ASIC for the ATLAS Level-1 Calorimeter Trigger* HD-KIP 00-13, Heidelberg, June 2000

[10] Xilinx Application Note 158 - Powering Virtex Devices `http://www.xilinx.com/xapp/xapp158.pdf`