ATLAS Level-1 Calorimeter Trigger: Subsystem Tests of a Jet/Energy-Sum Processor Module

J. Garvey, S. Hillier, G. Mahout, T. H. Moye, R. J. Staley, P. M. Watkins, A. Watson, R. Achenbach, P. Hanke, E.-E. Kluge, K. Meier, P. Meshkov, O. Nix, K. Penno, K. Schmitt, C. Ay, B. Bauss, A. Dahlhoff, K. Jakobs, K. Mahboubi, U. Schäfer, T. Trefzger, E. Eisenhandler, M. Landon, E. Moyse, J. Thomas, P. Apostologlou, B. M. Barnett, I. P. Brawn, A. O. Davis, J. Edwards, C. N. P. Gee, A. R. Gillman, V. J. O. Perera, W. Qian, C. Bohm, S. Hellman, A. Hidvegi, and S. Silverstein

***Abstract*—The ATLAS Level-1 Calorimeter Trigger consists of a Preprocessor, a Cluster Processor (CP), and a Jet/Energy-sum Processor (JEP). The CP and JEP receive digitized trigger-tower data from the Preprocessor and produce trigger multiplicities and total and missing energy for the final trigger decision. The trigger also provides region-of-interest information for the Level-2 trigger and intermediate results of the data acquisition system for monitoring and diagnostics by using Readout Driver modules. The JEP identifies and localizes jets, and sums total and missing transverse energy information from the trigger data. The Jet/Energy Module (JEM) is the main module of the JEP. The JEM prototype is designed to be functionally identical to the final production module for ATLAS and to have the full number of channels. Three JEM prototypes have been built and successfully tested. Various test vector patterns were used to test the energy summation and the jet algorithms. Data communication between adjacent JEMs and all other relevant modules of the JEP has been tested. Recent test results using the JEM prototypes are discussed.**

I. Introduction

AT THE FULL LHC design luminosity of 10^{34} cm^{-2}s^{-1}, there will be approximately 23 proton-proton interactions per bunch crossing. The ATLAS Level-1 trigger is to reduce the 40-MHz interaction rate to a trigger rate of 75 kHz for input to the Level-2 trigger. The reduction is performed by processing reduced granularity data from the calorimeters and muon spectrometer. Muon candidates are identified in a separate trigger.

In the Level-1 calorimeter, potentially interesting events are selected by identifying electron/photon candidates, jets, single-hadron/tau candidates, missing transverse energy, and total transverse energy. As shown in Fig. 1, the ATLAS Level-1 Calorimeter Trigger system [1] consists of three subsystems, namely the Preprocessor, electron/photon and tau/hadron Cluster Processor (CP), and the Jet/Energy-sum Processor (JEP). The latter two processor systems send results for every bunch crossing to the Central Trigger Processor (CTP), which makes a Level-1 Accept (L1A) decision based on them, including additional data from the Muon Level-1 Trigger system. If the CTP accepts the event, the processors read out more detailed information on the types and locations of event features [Regions of Interest (RoI)] and provides it to the Level-2 Trigger. The latency of the Level-1 trigger is limited to 2 μs. The system is built using custom designed, fast digital electronics. The ATLAS Level-1 calorimeter trigger processors use field-programmable gate arrays (FPGAs) as their main technology, which offer both the required performance and high flexibility.

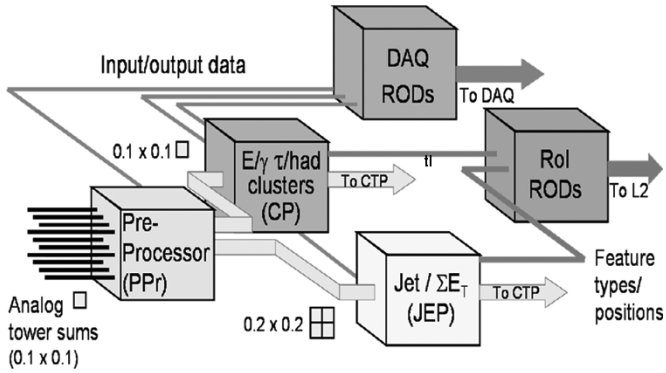

Fig. 1. ATLAS Level-1 calorimeter system.

This paper describes the JEP of the Level-1 calorimeter Trigger system, designed to identify and localize jets, and to sum total and missing transverse energy information. After a more detailed description of the Level-1 calorimeter trigger system, the architecture of the JEP will be described and standalone tests on real-time data will be presented. The integration of the JEP with other modules of the Level-1 trigger will be shown.

II. ATLAS Level-1 Calorimeter Trigger System

The calorimeter trigger covers the region $-4.9 < \eta < 4.9$ and $\phi = 0$ to 2π. On the detector, cells are combined to form trigger towers, with a reduced granularity of $\Delta\eta \times \Delta\phi = 0.1 \times$

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J. Garvey, S. Hillier, G. Mahout, T. H. Moye, R. J. Staley, P. M. Watkins, and A. Watson are with the School of Physics and Astronomy, University of Birmingham, Birmingham B15 2TT, U.K.

R. Achenbach, P. Hanke, E.-E. Kluge, K. Meier, P. Meshkov, O. Nix, K. Penno, and K. Schmitt are with the Kirchhoff-Institut für Physik, University of Heidelberg, D-69120 Heidelberg, Germany.

C. Ay, B. Bauss, A. Dahlhoff, K. Jakobs, K. Mahboubi, U. Schäfer, and T. Trefzger are with the Institut für Physik, Universität Mainz, D-55099 Mainz, Germany (e-mail: Thomas.Trefzger@uni-mainz.de).

E. Eisenhandler, M. Landon, E. Moyse, and J. Thomas are with the Physics Department, Queen Mary, University of London, London E1 4NS, U.K.

P. Apostologlou, B. M. Barnett, I. P. Brawn, A. O. Davis, J. Edwards, C. N. P. Gee, A. R. Gillman, V. J. O. Perera, and W. Qian are with the Rutherford Appleton Laboratory, Chilton, Oxon OX11 0QX, U.K.

C. Bohm, S. Hellman, A. Hidvegi, and S. Silverstein are with the Fysikum, University of Stockholm, SE-106 91 Stockholm, Sweden.

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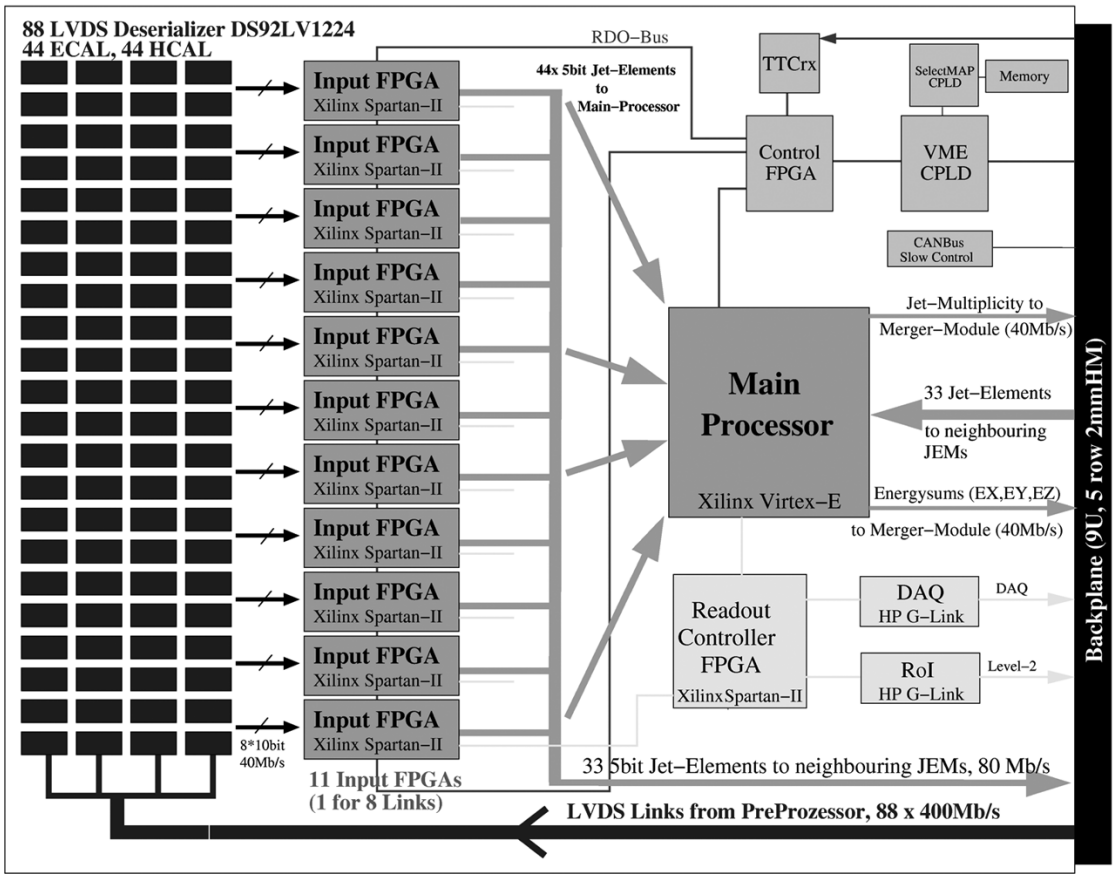

Fig. 2. Schematic architecture of a JEM, prototype version 0.1/0.2. One module uses a Virtex XCV600E device as Main Processor, the second one a Virtex XCV1600E.

0.1 over the region $-2.5 < \eta < 2.5$ for the CP and a granularity of $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$ for the JEP. Analog pulses enter the Preprocessor, where they are digitized to 10-bit precision at a frequency of 40 MHz. After bunch-crossing identification (BCID), the precise value of transverse energy for each trigger tower is produced in a lookup table. The transverse energy is an 8-bit word, giving a transverse energy scale up to 255 GeV. The total numbers of trigger towers is 7200. The CP and JEP receive digitized calorimeter trigger-tower data from the Preprocessor, and send trigger multiplicity information to the CTP via Common Merger Modules (CMM). Using Readout Driver (ROD) modules, the CP and JEP also provide region-of-interest (RoI) information for the Level-2 trigger, and intermediate and final results to the data acquisition (DAQ) system for monitoring and diagnostic purposes.

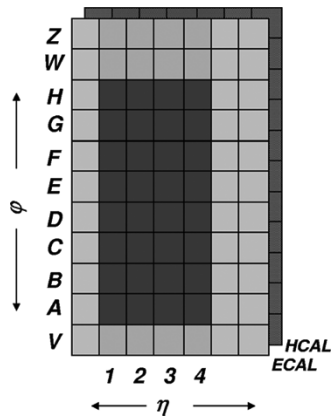

Fig. 3. Channel map of a JEM. Total range of input channels: 11×7 in $\eta - \phi$, of which 8×4 in $\eta - \phi$ are the core region.

III. Jet/Energy-Sum Processor

The JEP [2] must handle a large number of input signals and provide very fast logic. To minimize complexity of intermodule fanin-fanout caused by the use of sliding window algorithms, the system is subdivided into four quadrants, equivalent to the quadrants of the ATLAS calorimeters, which are each covered by a set of eight Jet/Energy Modules (JEMs). The sliding windows algorithm is a window grid that travels across the calorimeter until it has maximized the transverse energy seen in that same window. For reasons of cost and flexibility, the JEM uses programmable logic devices (FPGAs). All algorithms are developed, simulated and implemented using the hardware description language VHDL. The JEMs are purely digital modules, controlled via the VME interface. The architecture of a JEM is shown in Fig. 2.

Each JEM receives 88 data streams of 9-bit width via the serial links with each LHC bunch crossing (25 ns). These are the electromagnetic and hadronic components of jet elements in a $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$ grid. The receiving link chips de-serialize the data back to 40 MHz parallel words. In the 11 Input Processor FPGAs, the input electromagnetic and hadronic data are summed to form the 10-bit jet elements, which are then sent

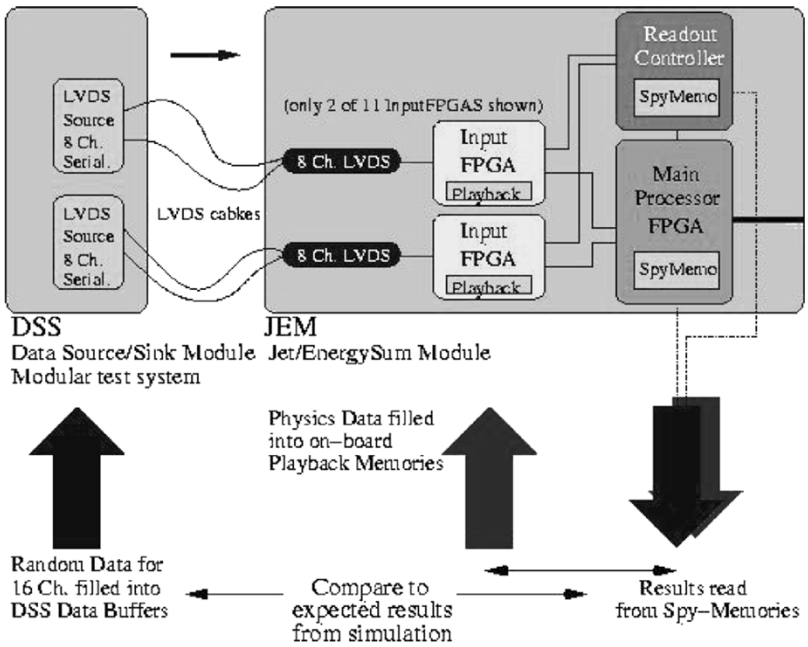

Fig. 4. Standalone test of the JEM with on board memories (playback and spy) and 16 channels of serial LVDS input.

to the JEM's central component, the Main Processor FPGA. The jet finding algorithm requires not only data from one JEM, but it also needs to correctly analyze jets crossing the JEM's boundary. Therefore, the jet elements are also copied to the neighboring JEMs via the backplane at 80 Mb/s. For the same reason, jet elements near the border of adjacent quadrants are duplicated in the Preprocessor and sent to JEMs in both quadrants. This results in a 11×7 grid in $\eta - \phi$ of jet elements available to the jet algorithms on one JEM. The energy sums are calculated from the jet elements of the 64 nonduplicated channels only (see Fig. 3).

The Main Processor calculates the local transverse energy (E_T) sum and the projections E_x and E_y of E_T in the X and Y directions for each $\Delta\phi$-bin.

These three energy values are coded to 8 bits, and sent from each of the 16 JEMs located in one crate to a CMM running firmware that forms the crate energy sums and ultimately the trigger sums that are sent to the CTP.

The jet algorithm identifies clusters of energy deposition within overlapping windows of adjustable size of 2×2, 3×3, or 4×4 jet elements. Jet locations are determined by looking for local maxima in regions of 2×2 jet elements. The total counts of jets above eight different programmable transverse-energy thresholds and window sizes are sent to another CMM running firmware that forms crate jet multiplicities and ultimately the sums over the full trigger that are sent to the CTP.

IV. Standalone Tests of Jet/Energy Module

Systematic tests [3] have been performed on the JEM prototypes in order to ensure correct and reliable operation of the JEM within the trigger environment. As a first step, the modules are operated stand-alone with the system clock provided by the onboard crystal oscillator, not by a Timing, Trigger, and Control (TTC) system. The playback memories of 256 words depth within the Input FPGAs are filled with various data patterns. A playback/spy cycle is initiated via a VME signal and the results from the spy memories are read back and compared to a full floating-point offline reconstruction algorithm for the energy summation. As a second step a Data Source/Sink (DSS) module has been used. The DSS, fitted with two Low Voltage Differential Signaling (LVDS) Source daughtermodules, provides a total of 16 serial LVDS channels and is able to serve two neighboring Input FPGAs with data, as expected from the Preprocessor system.

Fig. 4 shows the procedure of the standalone tests of the JEM.

A. Test Patterns

Two options of test patterns are available for JEM prototypes. The physics patterns, in this case the $t\bar{t} \rightarrow W^+W^-b\bar{b} \rightarrow$ Jets channel, were produced by the event generator PYTHIA [4] and then fed into the detector and trigger simulation ATLFAST [5] and ATL1CT [6]. 2.5 million events have been produced and stored for use in tests. Since a JEM covers only a very small area of space, an equivalent area which has more than 64 GeV of transverse energy depositions was written out by the trigger simulation. Since the deposition per event is very low, the kinematic cuts on the production level of PYTHIA have been set very high, in order to increase the rate of high energy jets within the data sample for the JEM: Mass 700–2000 GeV, transverse momentum $p_T > 500$ GeV.

Because of the high energy jets this set of test patterns requires all 64 channels of the core region (8×4 input channels in $\eta - \phi$) to be filled with data, which can always be achieved using the onboard playback memories.

Random patterns are also produced which cover the whole range of input data up to 9 bits (511 GeV) and are appropiate for those tests with a limited number of input channels of the JEMs. In order to increase the rate of high-energetic channels, but at the same time avoiding saturation, the channels are filled

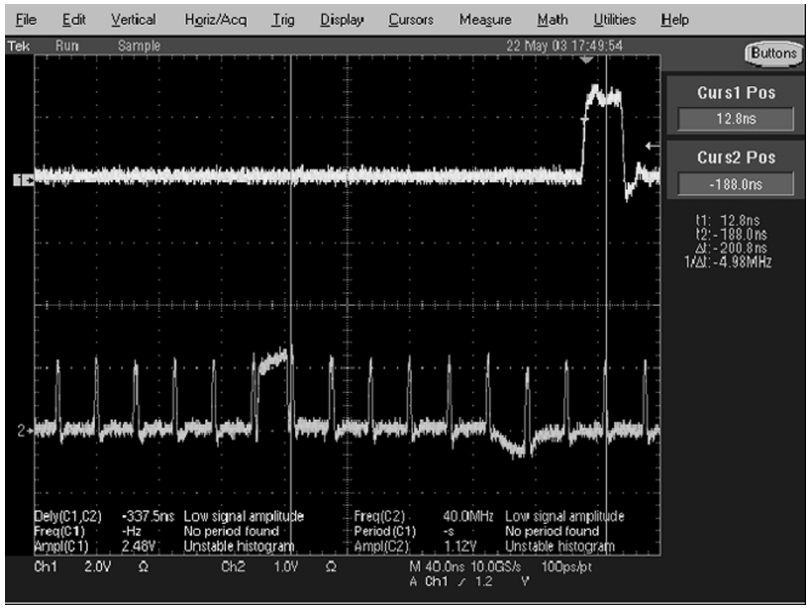

Fig. 5. Latency measurement of the real-time data path of the JEM prototype (energy summation only): total latency is eight bunch crossings (25 ns each).

using a random number between 0 and 1 folded with a sloping exponential function ranging from 0 to 511.

B. Test Using Playback and Spy Memories Only

Two JEM prototypes have been tested using the test vector patterns described above. A test was performed using the $t\bar{t}$-event library, processing the library 24 times, with a total of 60 million events. The results for the energy summation algorithm for ΣE_x, ΣE_y and ΣE_T were identical to the expected values from the offline summation. Another test used random patterns. A total of six million events was processed, also showing the expected results for the energy sums.

C. Test Using 16 Channel Serial LVDS Input Data From DSS and Spy Memories

The test was then extended using a DSS module fitted with two LVDS Source daughtermodules, which provide a total of 16 serial LVDS channels, being able to serve two neighboring Input FPGAs with data as expected from the Preprocessor system. Due to the limited number of channels, the random patterns described above have been used in this test. For this test, the data buffers in the DSS (depth 32 k words) are filled repeatedly with the random test vectors. The DSS is set to send a constant stream of data. A VME signal enables the spy memory inside the JEM's Main Processor to be filled. The data is then read back from this memory, matched with the repetitive stream and compared with the expected results. This setup processed 1.8 million events and all received values for the energy sums were as expected. The test has been repeated using all four possible pairs for Input FPGAs in the core region.

D. Loopback Test of Duplicated Channels

In order to test the connectivity of the backplane, a loopback device has been designed, feeding the outputs of jet element data from the Input FPGAs intended to go to the neighboring JEM back into the Main Processor of the same JEM. The energy summation algorithm is changed to accept the duplicated channels instead of the core region. A test pattern of a binary counter is used to check the correct reception of the data, which has been found to work properly.

V. Test of Jet/Energy Module With LVDS Data Feed Within ATLAS Software Environment Controlled by TTC

The test setup for the JEM prototype was then extended with a TTC system for system clocking and command distribution. A daughtermodule housing a TTCrx chip is mounted on the JEM prototype. A TTC system consisting of a TTCvi and a TTCvx module [1] is connected to the JEM via the electrical output and to the DSS via the optical output. Whereas the tests described in the previous paragraph have been controlled by simple test scripts and programs based on the VME driver routines, all further tests have been carried out using routines in C++ within the Level-1 Calorimeter Trigger software environment.

The Linux installation of RedHat 7.3 on the VME single board computer includes the ATLAS online software package and the CERN VME driver. The Level-1 Calorimeter Trigger software is installed, which includes all necessary routines to initialize, configure, and control the hardware as well as the simulation. The routines dealing with the hardware directly, the *ModuleServices*, are developed by the responsible groups as well as the simulation *ModuleSim*, which are being developed for each module, very closely modeling the functionality of the modules. The simulation is run in parallel in an identical setup as the hardware. This setup is described by database files using XML, which include all information about module types, crate location of modules, cables, and connections. The test setup is controlled by the *RunControl*. The firmware of the Input FPGAs

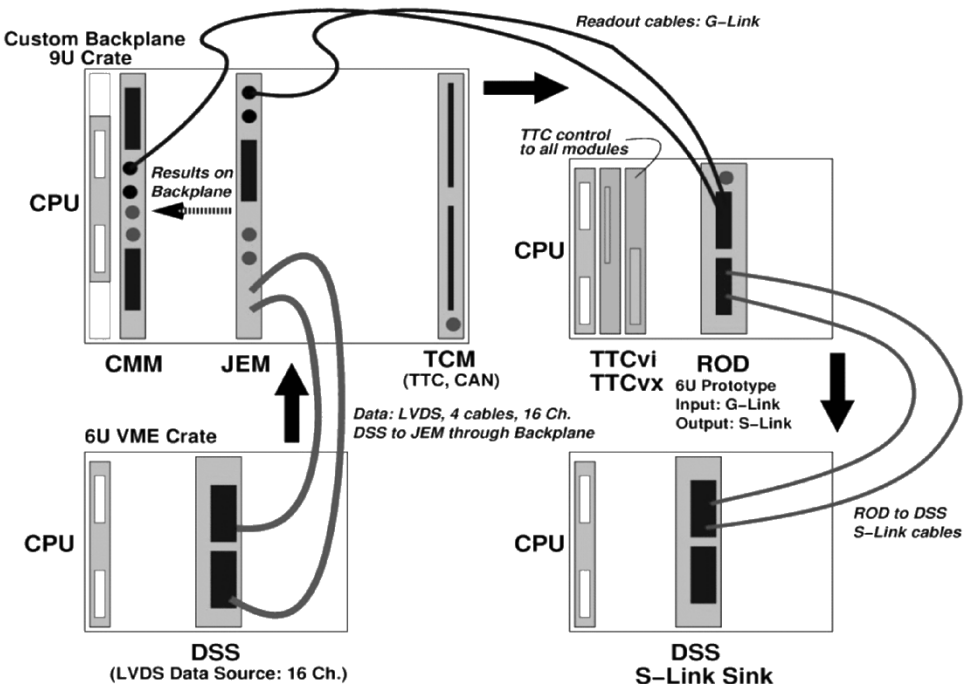

Fig. 6. Readout of JEM with DSS as LVDS data feed, Readout Driver, and DSS for S-Link data sink.

is supplemented with an input synchronization stage, which ensures a reliable data transfer at the input stage of the JEM by adjusting the clock phase of the internal DLLs of the Xilinx Spartan-II FPGA in order to allow for compensation of delays between the input channels caused by cables and onboard tracks and routing. One of the four available clock phases of the DLLs is automatically selected when a special synchronization pattern is fed to the Input FPGAs.

The tests described in the previous chapter have been repeated with this setup, using both the random and the physics test patterns. System commands for playback/spy cycles are broadcasted using the TTC system. The results read back from the spy-memories of the Main Processor have again been found to be identical to the expected values from the simulation. The main jet algorithm has been implemented into the JEM prototype's Main Processor, but the results are different from the expected values of the simulation. Therefore the implementation is being reworked, allowing to fit the algorithm into the present devices by optimization of the VHDL code structure. The algorithm has been successfully simulated and run in a standalone environment.

The readout functionality of the module was tested in a standalone setup using a spy-memory within the readout controller, that captures all readout data streams from the Input and Main Processor FPGAs. The data has been found to match the expected data packets. Further tests using the complete readout chain are described in the following paragraph. Using the two available JEM prototypes mounted into the custom backplane within the 9U crate, a latency measurement has been done. The deskew 2 setting of the TTC is used for this scan. The latency of the JEM algorithm has been found to be eight bunch crossings (25 ns each). A capture from the oscilloscope illustrating the latency is shown in Fig. 5.

VI. Trigger Prototype Module Integration: Readout of the JEM

All interfaces of the JEM to the outside world within the experiment environment are tested in an integration test. The setup is illustrated in Fig. 6. Input data as expected from the Preprocessor is fed into the JEM using a DSS module with 16 channels of serial LVDS source. The results of the JEM are transmitted via the custom backplane to the CMM. The outputs of both the JEM and the CMM are transmitted via G-Link cables connected to the prototype Readout Driver, which converts the readout data packets for transmission via S-Link cables. The data sent through the S-Links is received by a DSS equipped with an S-Link sink module. Using this setup, incoming data and results at all interface stages of the system can be checked both by comparing the readout data and also by using the spy memories inside the modules. In order to ensure a consistent set of data from the various stages, the readout signal is provided by the TTC system, which is also used to provide all system clocks. The system has also been tested for the whole number of input channels using the playback memories of the JEM's Input FPGAs. The expected S-Link output data is generated by the simulation chain. Both sources of input data—either the DSS's data buffers or the Input FPGA playback memories—are filled using the very same data patterns as the online trigger module simulation, allowing for an automated comparison of the readout streams.

VII. Development of Final JEM for ATLAS

Based on the positive results of this program, the final JEMs (Module 1) will be designed in 2003. Volume production of the 32 JEMs needed for ATLAS will start in 2004. The next generation of the JEM is planned to be the module to be used in the

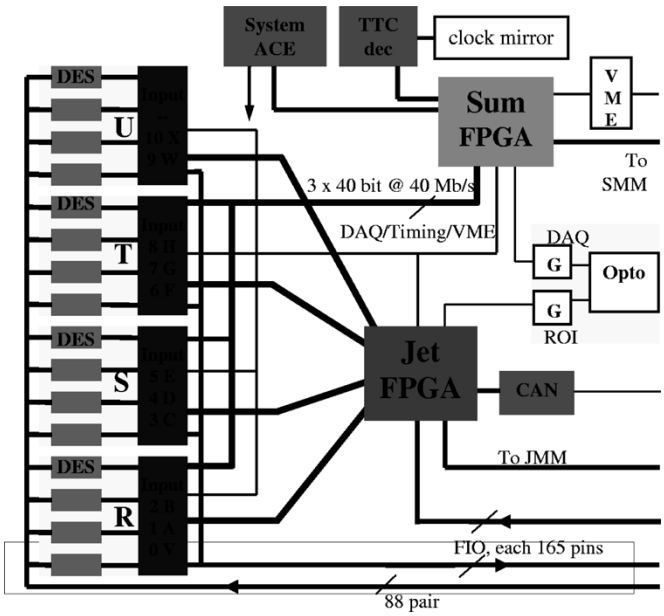

Fig. 7. Final JEM for ATLAS.

final ATLAS Level-1 Calorimeter trigger. It is being designed taking into account the experiences from the tests of the prototype modules and the development in technology. A schematic overview of this module is given in Fig. 7. LVDS deserializer devices of the SCAN series [7] are used, which will allow for JTAG/Boundary scan testing of the onboard connections. Each of those devices deserializes six data channels. A new generation of FPGAs, the Virtex-II [8] series, has become common and will be used on JEM-1. They offer higher logic densities and improved performance. Since fine-pitch ball grid array packages are usually fitted to smaller printed circuit boards in the current commercial market, it has been decided to fit one Input FPGA and four LVDS deserializers on daughtermodules. A JEM-1 will be fitted with four of those daughtermodules. The use of daughtermodules also simplifies the rework of faulty modules significantly, as they can be easily replaced. The readout and control functions will also be on a daughtermodule, leaving basically only the Main Processor mounted on the mainboard of JEM-1. The firmware has been updated to match the new devices and mapping. Since all interfaces to the outside world are identical, Module-1 can replace the current prototype in the module integration tests. The daughtermodules and the mainboard are under production and will be subjected to standalone tests and module integration tests in 2004.

VIII. Conclusion

Two fully functional JEM prototypes have been designed, produced, and tested in a stand-alone test setup using test vectors for the energy sum algorithm. Test vectors were generated by the trigger simulation, which provides both input data for the JEM and the expected energy summation results. Since all stand-alone tests of the electronics modules have been successful, two JEMs are being subjected to system tests in a setup simulating the final ATLAS environment. These measurements allowed for thorough tests of all interfaces of the JEM to the outside world, encompassing both the physical interfaces as well as the software integration. A complete set of LVDS sources, the final backplane, the Timing and Trigger distribution system, and the Readout System were available. Based on the results of this program and recent developments in technology and board manufacturing, the final JEM is being designed. Volume production of the 32 JEMs needed for ATLAS will start in 2004.

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