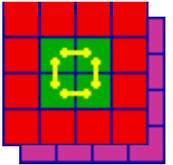




Pre-Production Validation of the ATLAS Level-1 Calorimeter Trigger System



ATLAS Level-1 Calorimeter Trigger Collaboration:



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³CCLRC Rutherford Appleton Laboratory, Oxon, UK

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⁵Physics Department, Queen Mary, University of London, London, UK

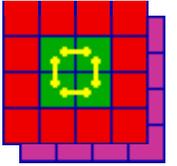
⁶School of Physics and Astronomy, University of Birmingham, Birmingham, UK



Validation of ATLAS Level-1 Calorimeter Trigger, Stephen Hillier



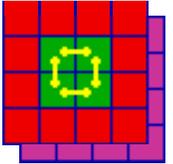
Pre-Production Validation of the ATLAS Level-1 Calorimeter Trigger System



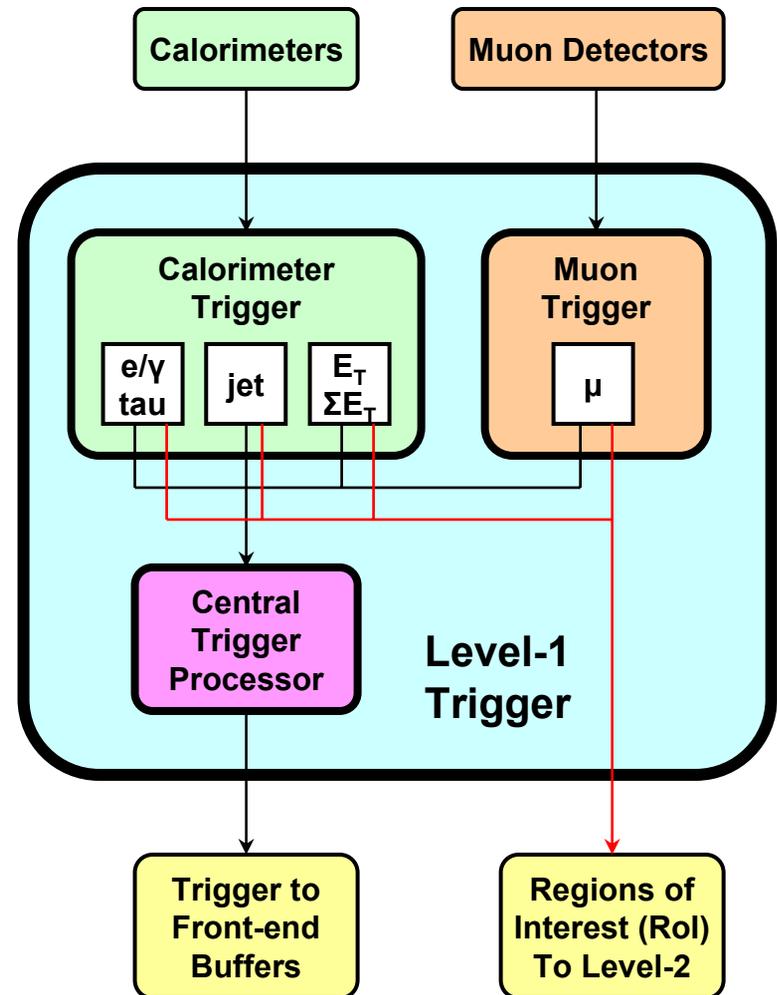
- Trigger Architecture
- Module Design and Challenges
- Testing Methodologies:
 - Software data verification
 - Real-time link stability measurements
 - Test-beam performance



Level-1 triggering in ATLAS

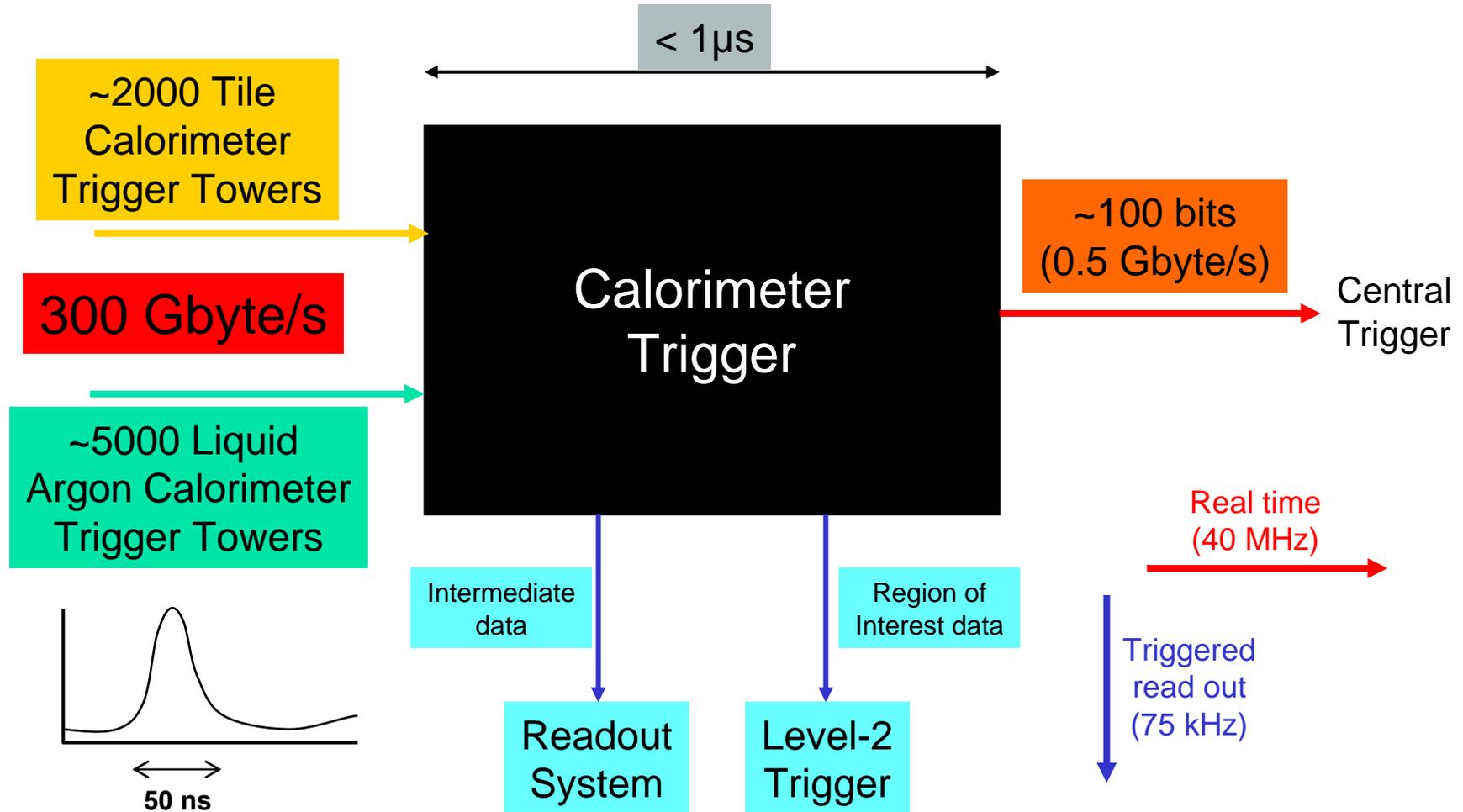
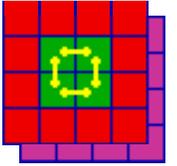


- All data buffered at bunch-crossing rate of 40 MHz for 2.5 μ s
- Three-stage triggering system
 - Level-1: custom built hardware, fixed latency - target rate 75 kHz
 - Level-2: software, RoI based selection - target rate 1000 Hz
 - Event Filter: software, full detector - target rate 200 Hz
- Level-1 has three sub-systems:
 - Calorimeter Trigger
 - Muon Trigger
 - Central Trigger (CTP)



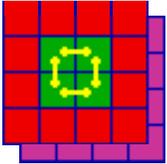


Calorimeter Trigger Requirements

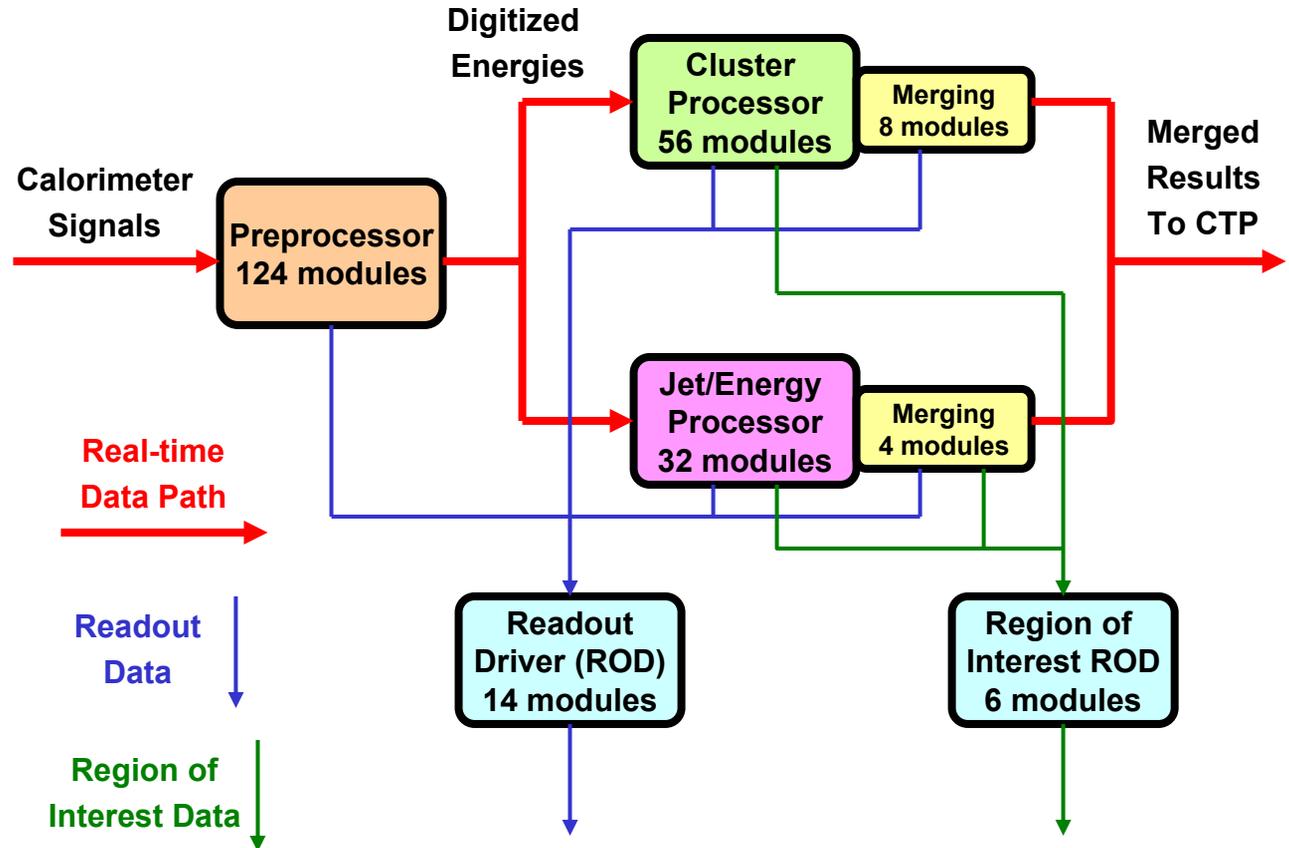




Calorimeter Trigger Architecture



- Features:**
- Realtime Path: Fixed Latency Pipelined
 - Many stage processing
 - Massive parallelism
 - Dual purpose modules
 - Heavily FPGA based

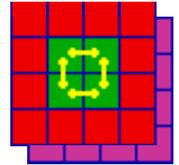


Five Types of Custom 9U Modules

PPM	CPM	JEM	CMM	ROD
-----	-----	-----	-----	-----



Generic Module Design



Challenges:

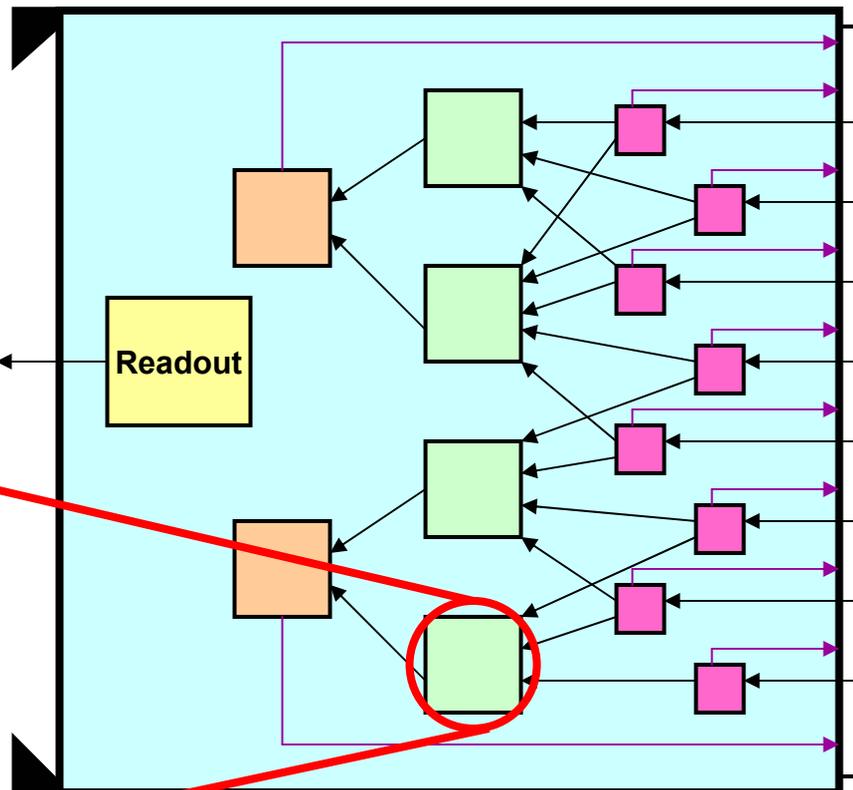
- Many FPGAs
- High connectivity
 - Internal
 - External (via backplane)
- High speed signals

Merging Stage
1-2 FPGA

Processing Stage
1-8 FPGA

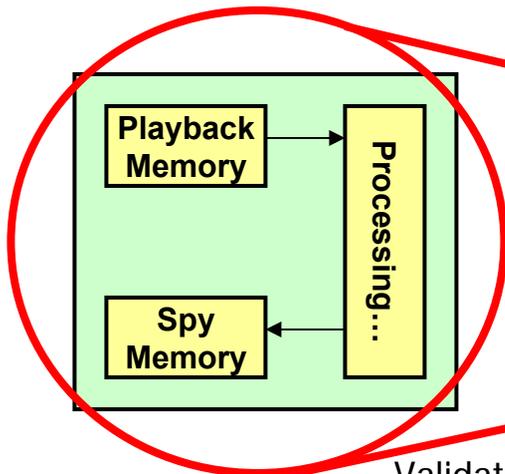
Input Stage
1-20 FPGA

Readout output up to 800 Mbit/s



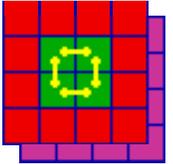
High Density Back-plane Connector (~1150 pins)

Signal Speeds up to:
400 Mbit/s differential
160 Mbit/s single ended



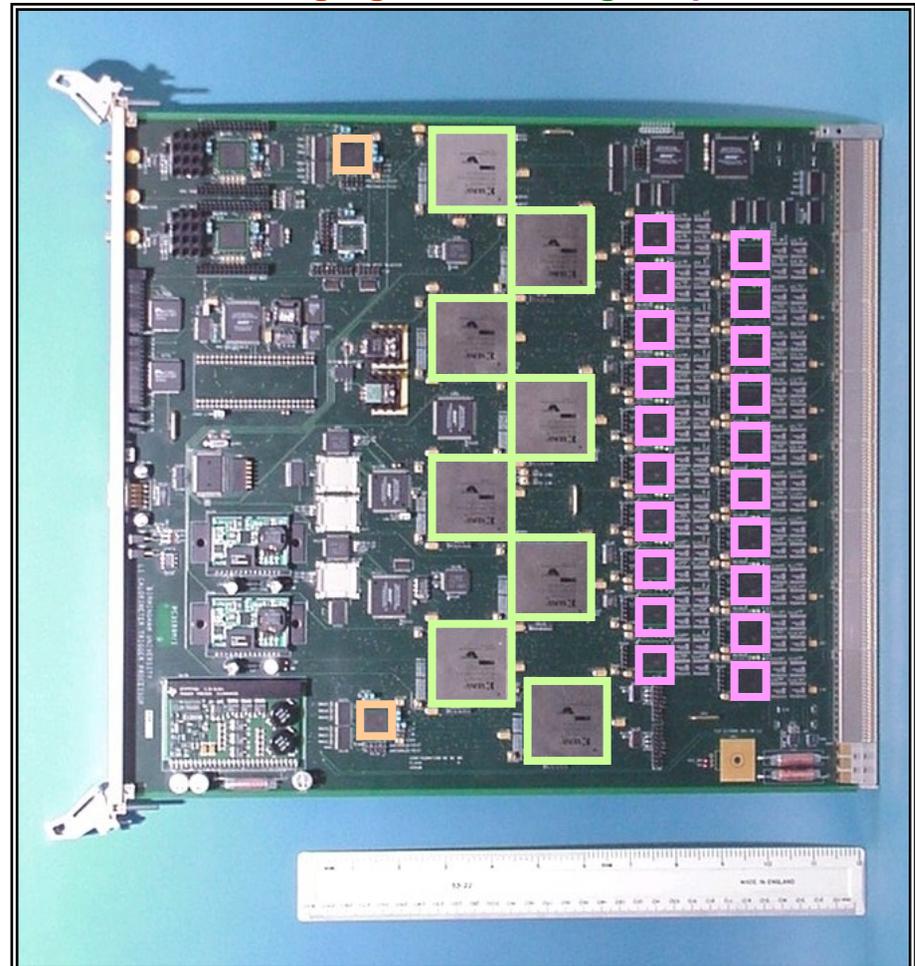


A real example: the Cluster Processing Module



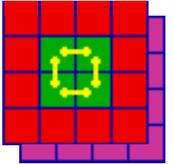
- Backplane Connector i/o
 - Input: ~58 Gbit/s
 - Output: ~28 Gbit/s
- Input Stage:
 - 20 FPGAs
- Processing Stage:
 - 8 FPGAs
- Merging Stage:
 - 2 FPGAs
- **Modules Needed: 56**

Merging Processing Input





Module Testing Goals and Tools



- High speed link stability and performance
 - Use data integrity to establish good timing windows
 - High statistics mode measurements in real-time
 - Parity error counting
 - Dedicated firmware loads

- Algorithm correctness
 - Use specially designed test-vectors, eg:
 - Physics-like
 - Boundary conditions

- Data formatting
 - Read-out must conform to external expectations

- System Integration
 - Does the complete chain work as a trigger?

Detailed Module Simulation

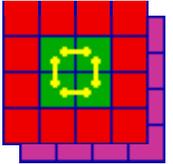
Runs in parallel with hardware
Predicts output data at any stage
Requires generation of synchronised trigger patterns

Test-beam operation

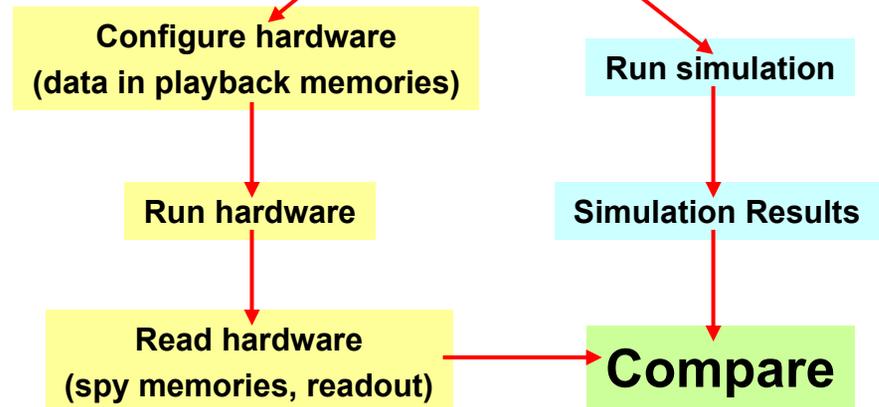
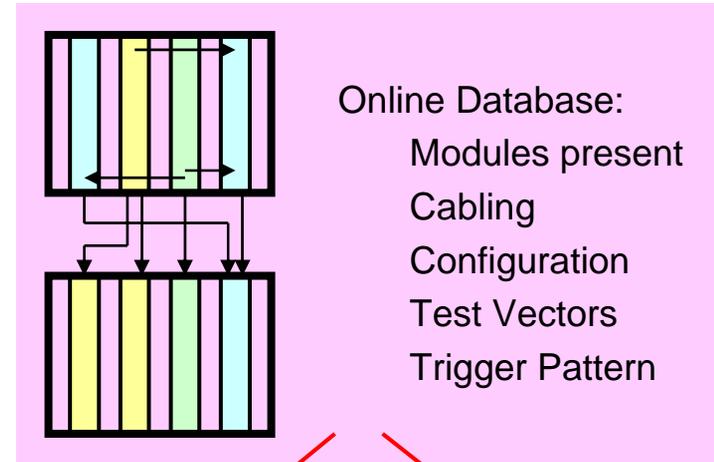
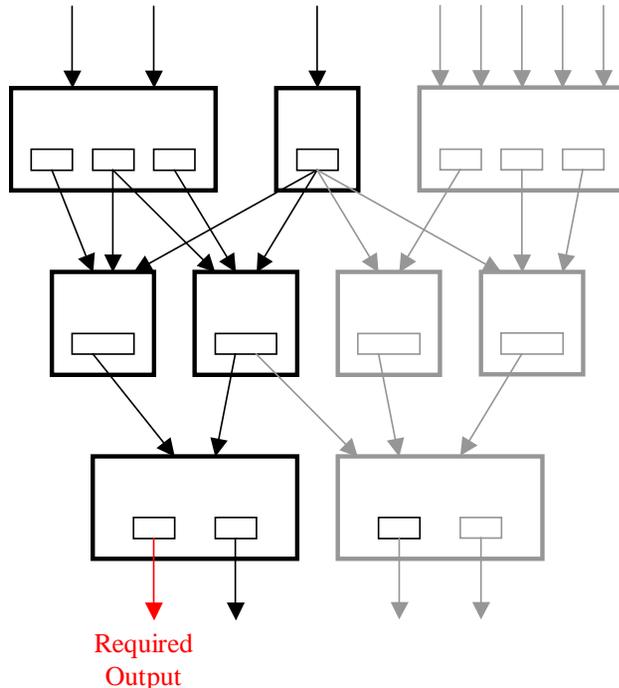
Analogue inputs vs Calorimeter data
Digital processing integrity



Simulation architecture and usage

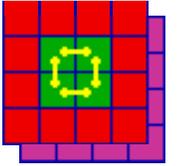


- Generic C++ framework
- VHDL inspired
 - Processes, Ports, Links
- Hierarchical, Scalable
- Output 'Driven'





Artificial trigger generation

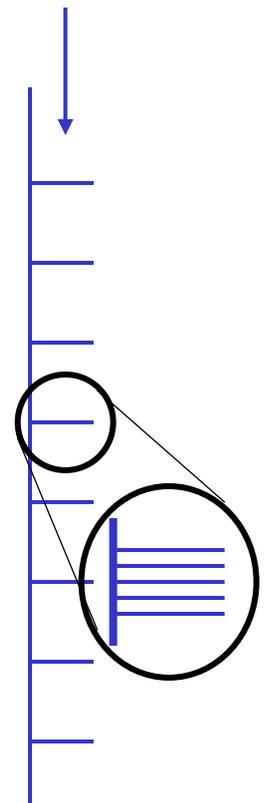


- To predict readout data need to control trigger generation
- Also need to test hardware with high rate and 'difficult' trigger patterns
- Done via a custom module plus trigger pattern generation (under user control)
- Triggers synchronised to playback memories
- Simulation also knows about trigger pattern
- Many types of pattern possible

Continuous:
eg 50 kHz

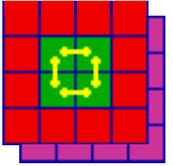


'Bursty': eg
Bursts of 5
triggers

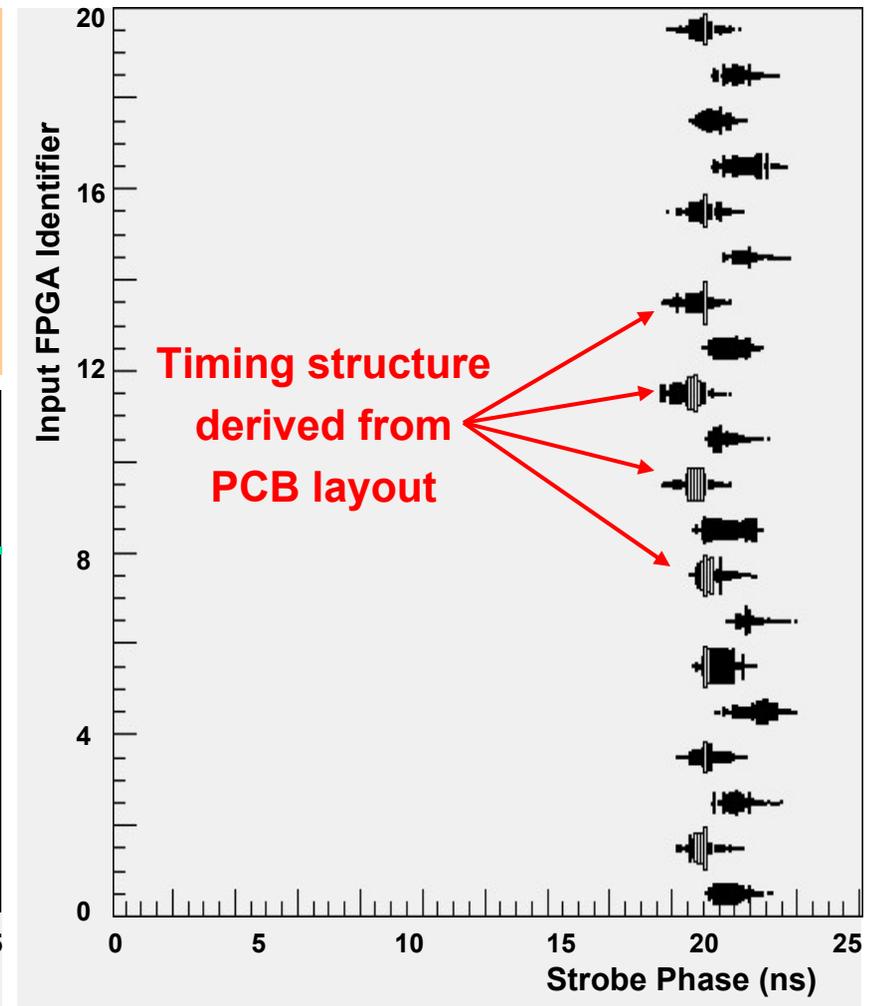
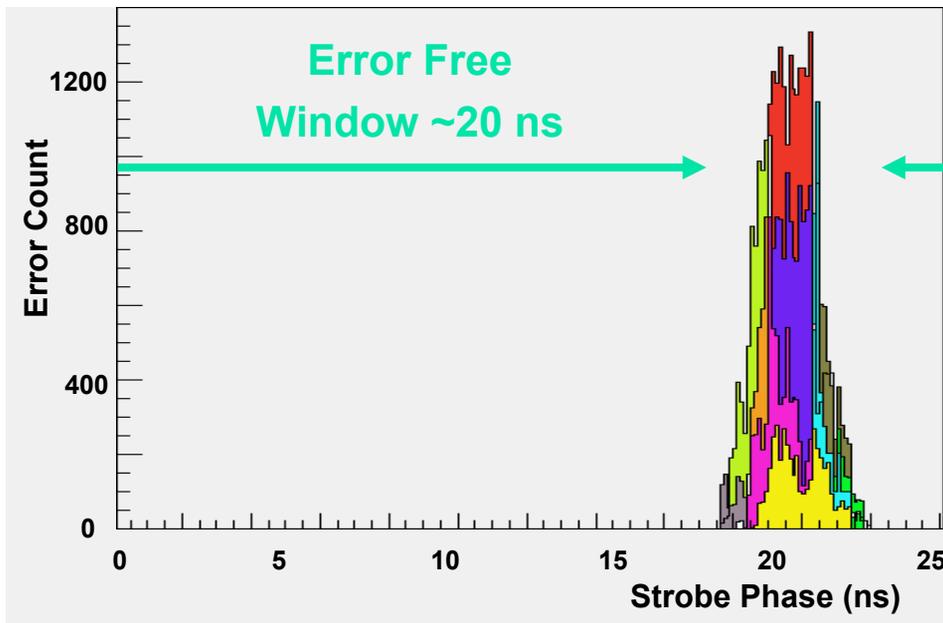




CPM input LVDS timing windows

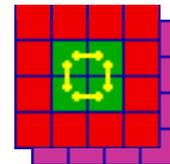


- Input FPGAs receive 40 Mbit/s signals
- Input strobing requires timing
- Timing window: 20ns over whole module
- Once optimised, check with firmware
 - No error in 10 minutes in whole module = bit error rate < 1 in 10^{13}



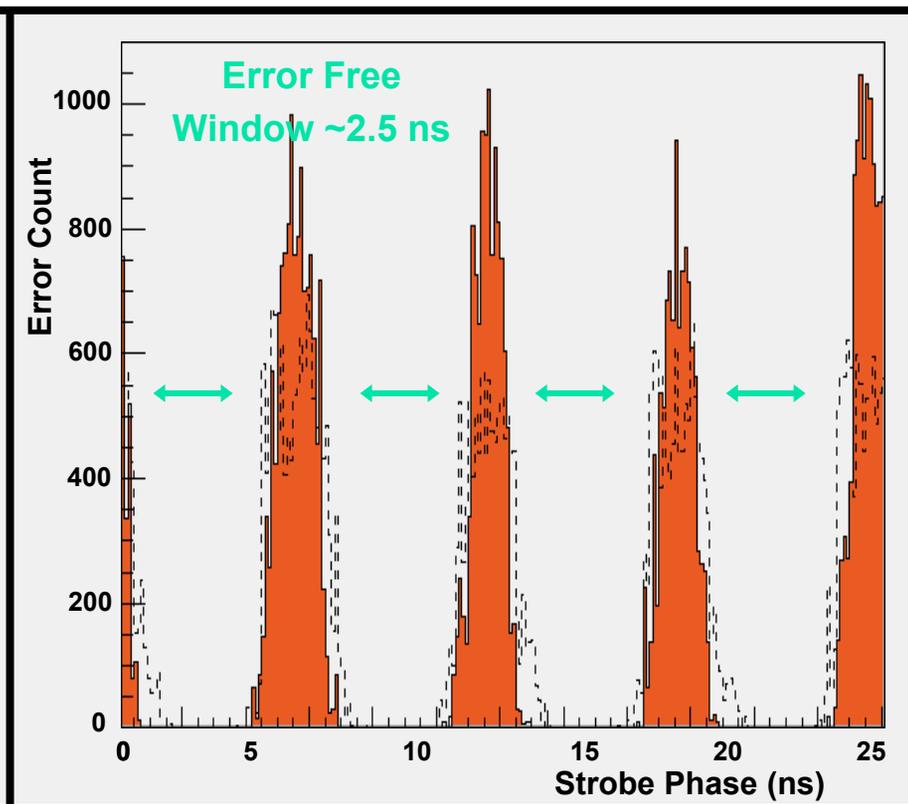
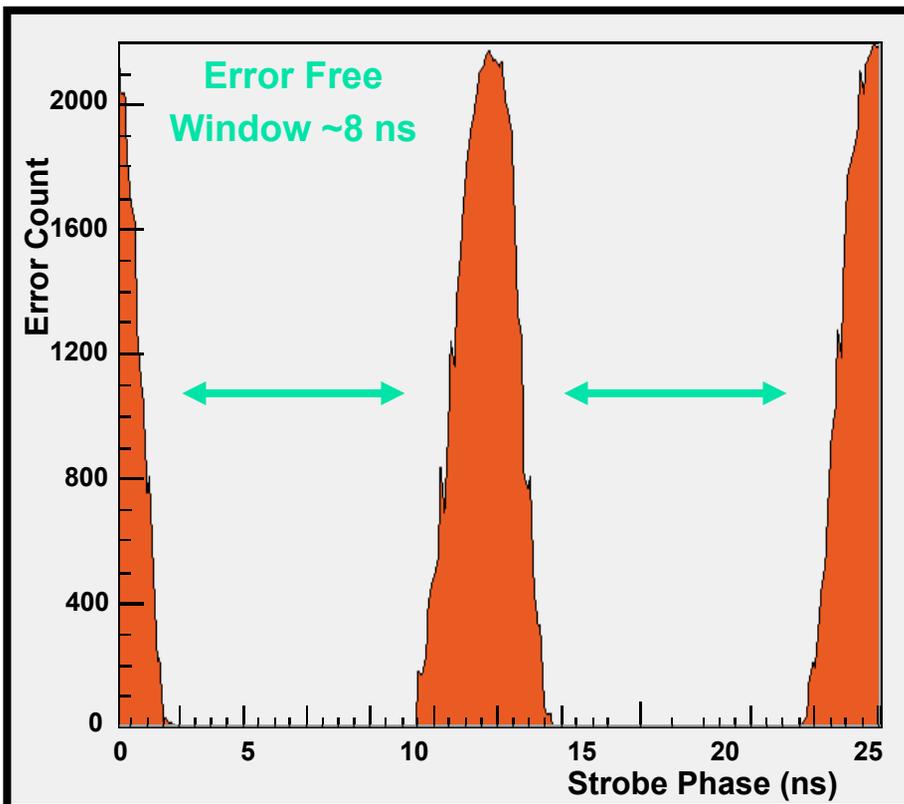


Processor FPGA timing windows



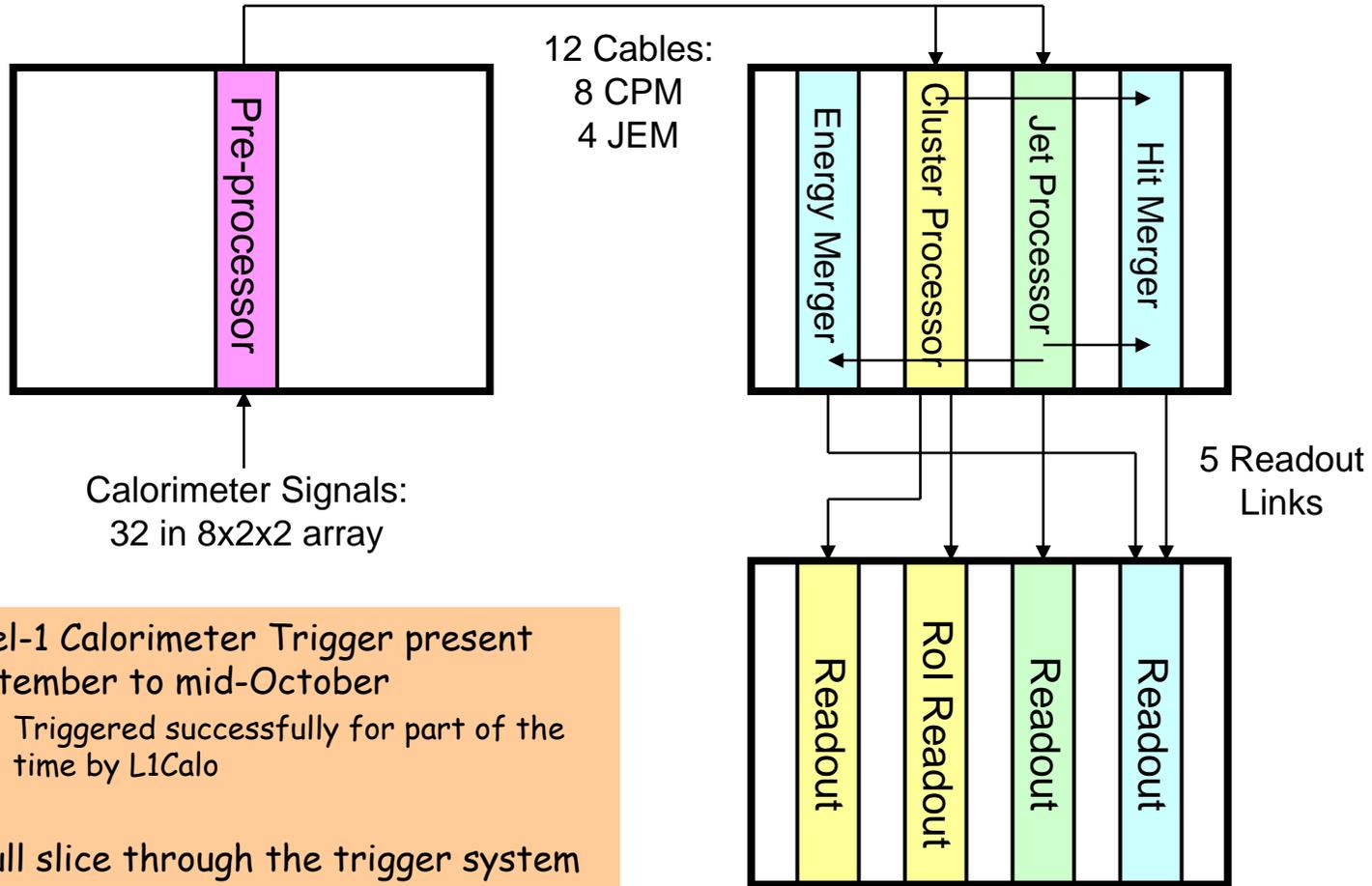
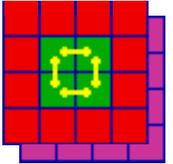
- Jet/Energy Processor FPGAs:
385 inputs at 80 MHz
210 on-board, 165 from backplane

- Cluster Processor FPGAs:
108 inputs at 160 MHz
60 on-board, 48 from backplane





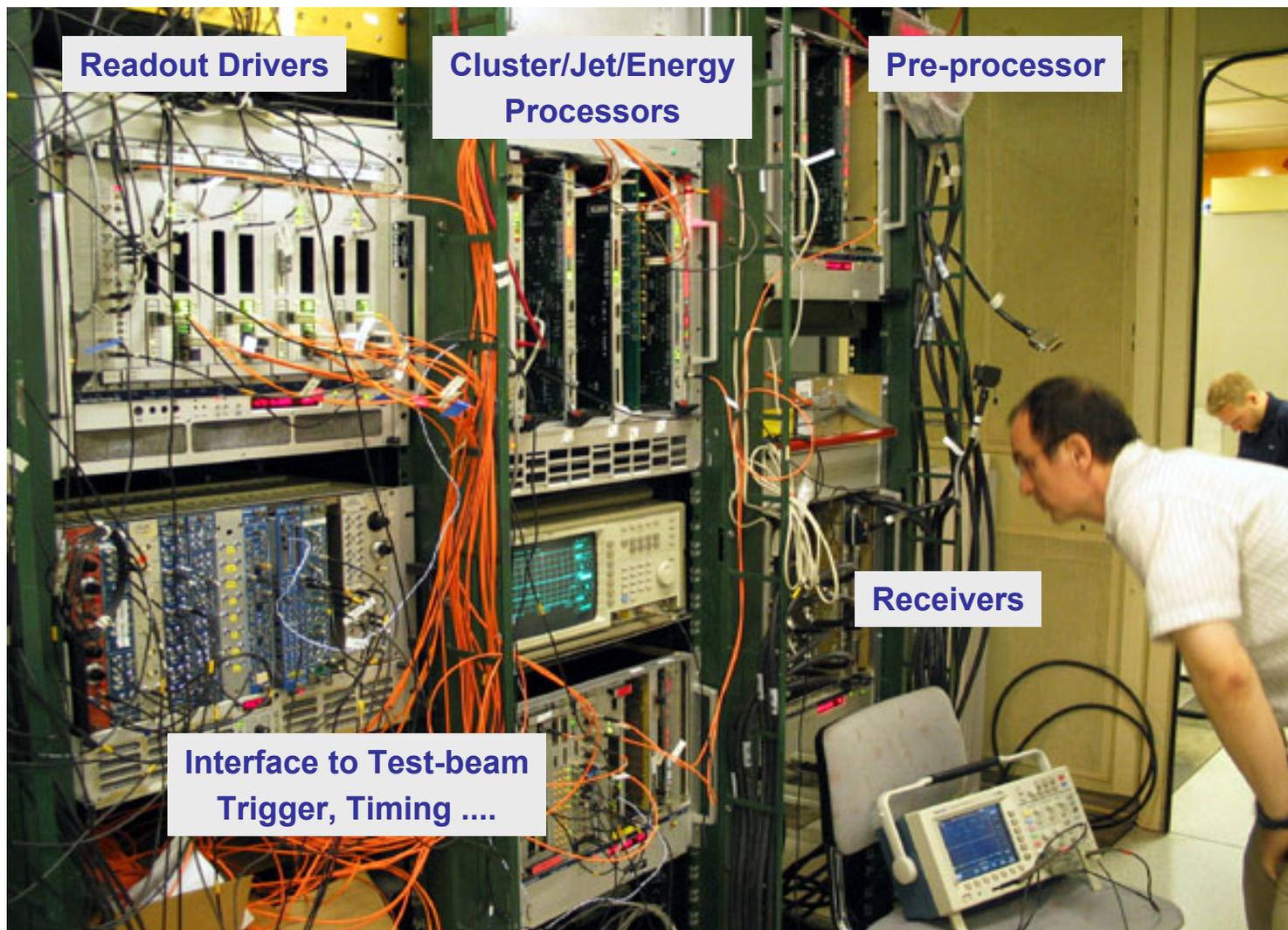
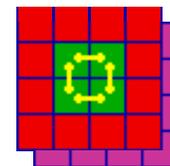
ATLAS Combined Test-beam 2004



- Level-1 Calorimeter Trigger present September to mid-October
 - Triggered successfully for part of the time by L1Calo
- A full slice through the trigger system
 - ~1% of final capacity



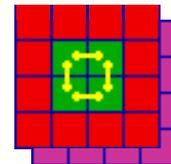
The Reality



Validation of ATLAS Level-1 Calorimeter Trigger, Stephen Hillier



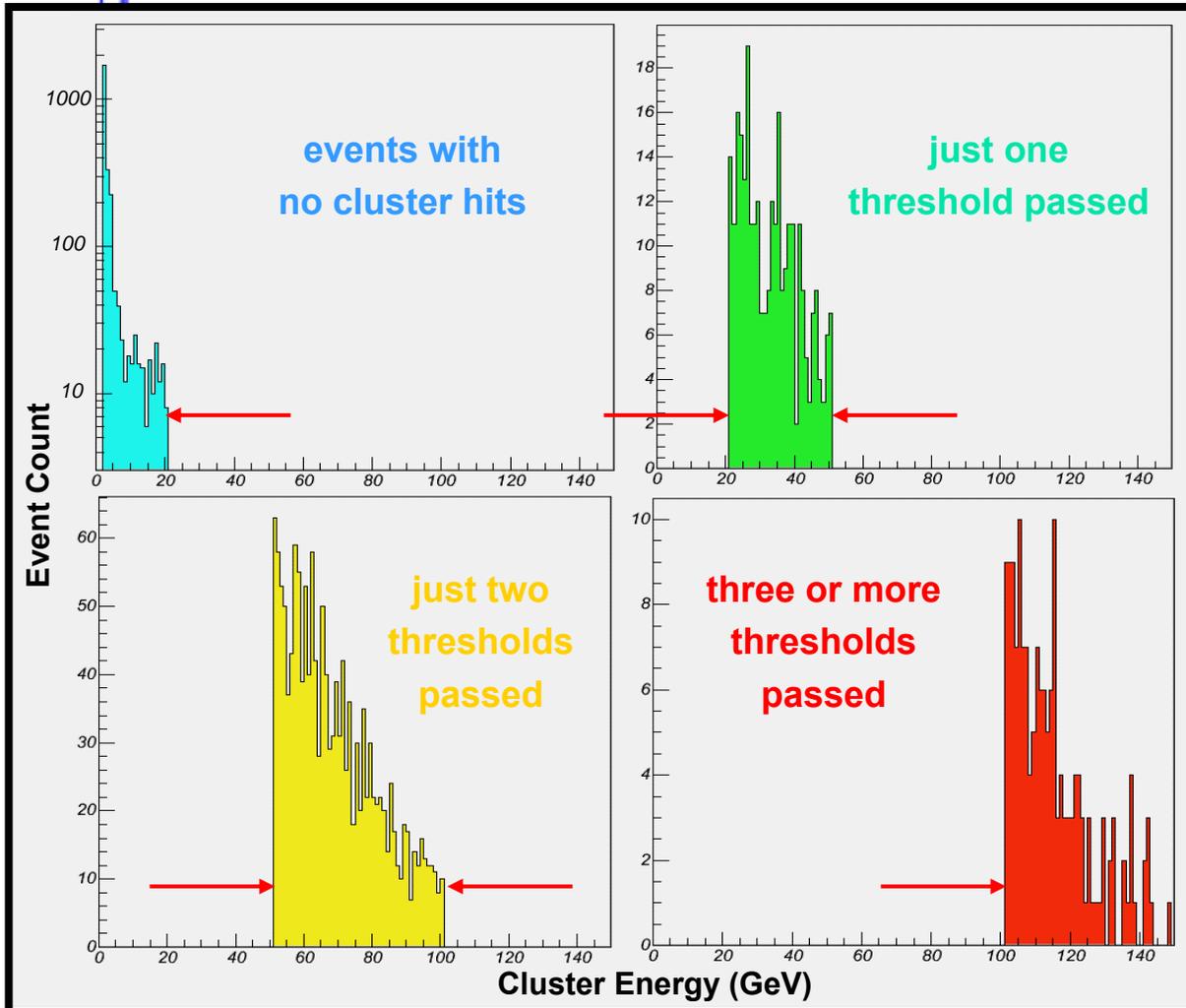
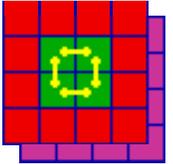
Checks on Test Beam data



- Internal Consistency checks
 - Assume full granularity input data is correct
 - Are all other data (energies, hits etc) consistent?
 - Performed in ~500,000 events
 - Only minor problems, identified as firmware features
 - No evidence of data integrity problems
- Comparisons with Calorimeters
 - Good correlation was seen
 - With some problems - overlapping pulses?
 - Triggers generated on genuine physics events



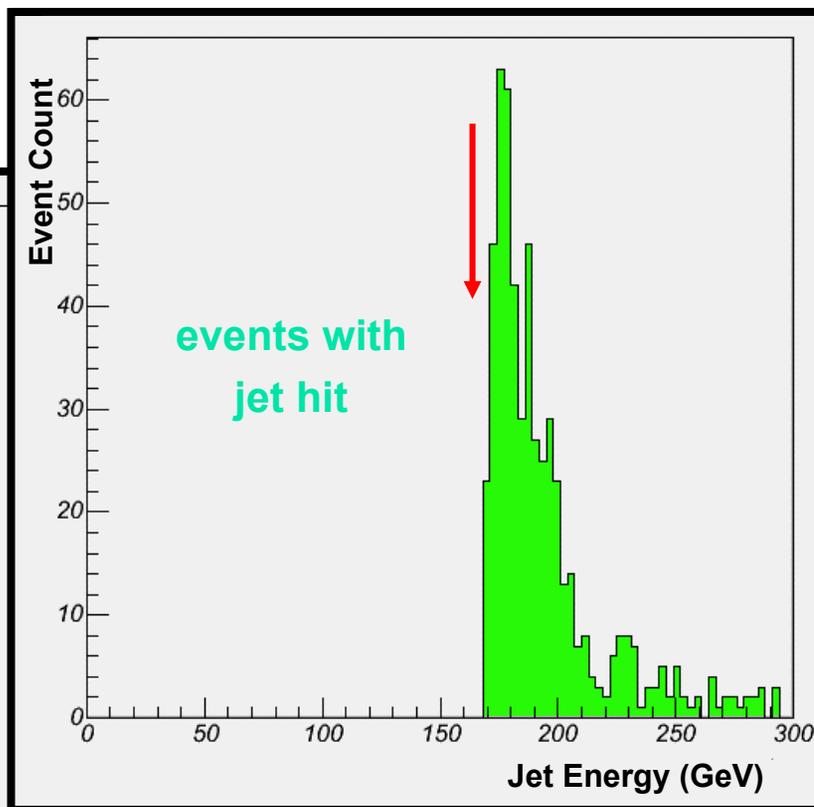
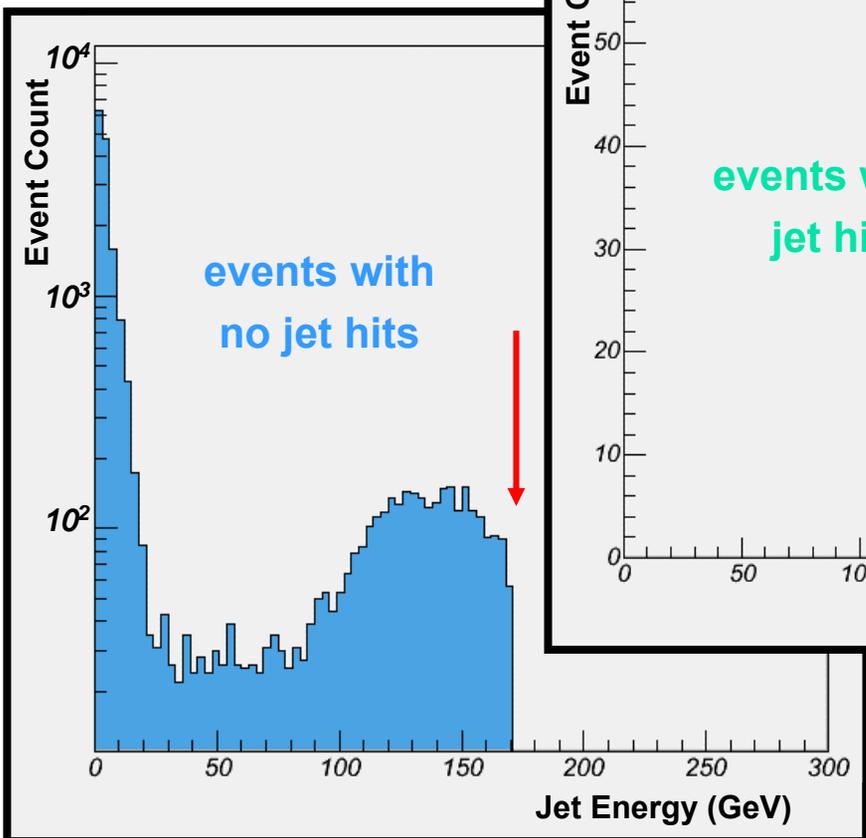
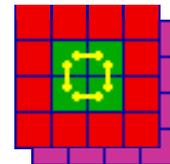
Cluster processor hit results



- Four thresholds
 - 20, 50, 100, 200 GeV
- Hit results are as expected
- RoIs also checked
- Positions, hits all formed correctly



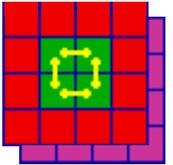
Jet/energy algorithm results



- Only one threshold used
 - 170 GeV
- No errors seen in hits
- No errors seen in energy sums



Correlation with calorimeters

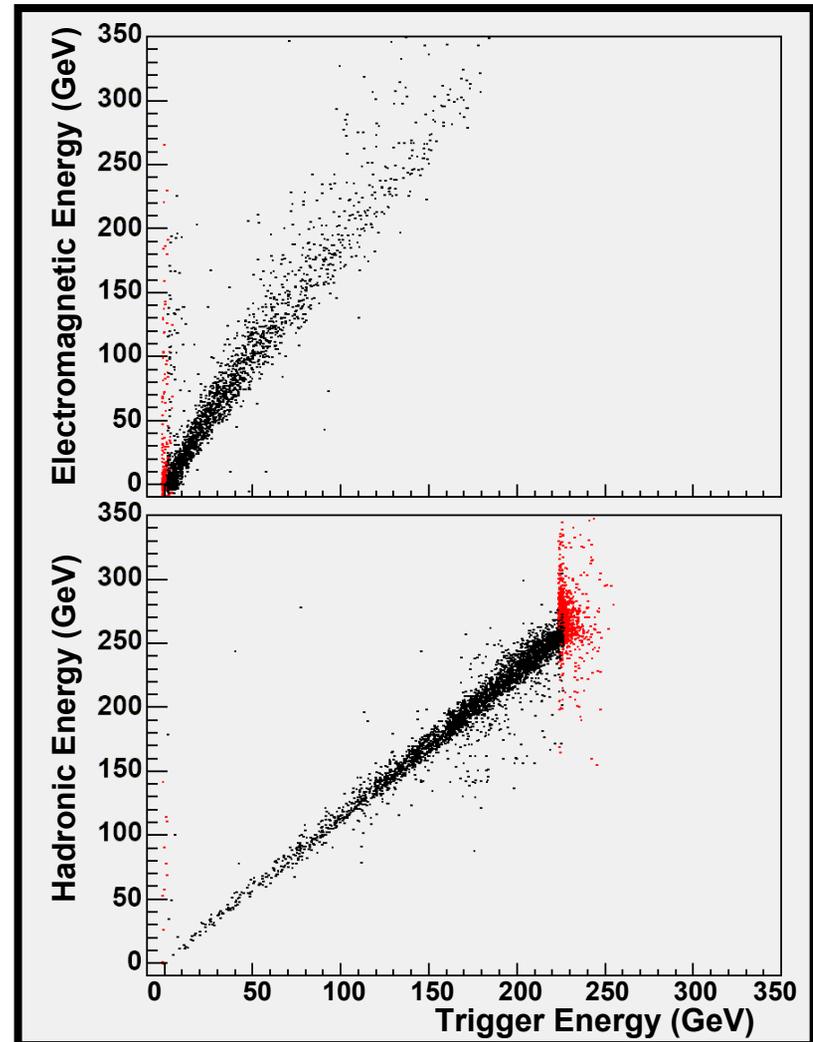


o Liquid Argon comparison:

- o ~factor 2 scaling (ET)
- o Lose energy in some events: overlapping events? bunch-crossing identification problem?

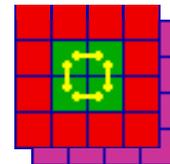
o Tile comparison:

- o Very encouraging
- o Saturation at ~ 225 GeV understood





Did the Trigger Work?



- Run with Cluster Threshold of 20 GeV as CTP trigger
- Clear cut-off in Electromagnetic Energy as Measured by Liquid Argon Detector

