Large scale production of the Multi-Chip Module of the ATLAS Level-1 Calorimeter Trigger

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Abstract

The Multi-Chip Module (MCM) is the main processing block of the Pre-Processor System in the ATLAS Level-1 Calorimeter Trigger. The MCM holds a dedicated signal-processing ASIC and a Phos4 timing-chip together with seven commercial dice mounted on the substrate. Those are four FADCs and three LVDS-serializers.

The MCM contains the main functionality of the Pre-Processor System, namely the digitization, calibration and Bunch-Crossing-Identification of calorimeter signals. Two output data streams are produced by the MCM. A real-time stream transmits the processed data to the subsequent trigger processors. A readout stream provides readout information of the Pre-Processor.

The MCM is the smallest exchangeable unit of the Pre-Processor. The ATLAS experiment will have 2048 MCMs installed in the Pre-Processor system. Including spares, the total number runs up to 3000. The production phases of the MCMs and test procedures for quality control at different stages of the production are presented.

I. Introduction

The ATLAS trigger system is based on three levels of event selection. These levels are the Level-1 Trigger, the Level-2 Trigger and the Event Filter. The trigger system reduces the initial bunch-crossing rate of 40 MHz to the rate of selected events of 200 Hz. The first selection step is performed by the Level-1 Trigger system , reducing the initial event rate to about 75 kHz [1]. The Level-1 Trigger consists of three building blocks - the Calorimeter Trigger, the Muon Trigger and the Central Trigger Processor (CTP). The Calorimeter Trigger receives about 7200 analog signals from electromagnetic and hadronic calorimeters, summed in projective Trigger Towers (TT) with a reduced granularity in $\eta \times \phi$ of 0.1x0.1. The results from the Calorimeter Trigger together with those from the Muon Trigger are sent to the CTP, which generates the final Level-1 Trigger decision.

The Level-1 Calorimeter Trigger consists of three subsystems: The Pre-processor (PPr), the Cluster Processor (CP), and Jet/Energy-sum Processor (JEP). The Pre-processor receives the analog input signals from all ATLAS calorimeters, digitizes and synchronizes them; in addition it performs the bunch-crossing identification (BCID) and uses a lookup table to calibrate the transverse energy (ET). The digitally processed data are then transmitted to the CP and JEP subsystems. The CP subsystem identifies possible isolated electrons, photons and semi-hadronic τ decays. The JEP subsystem identifies jet objects and calculates the global sums for the E_T-miss and sum-E_T triggers. The multiplicities of objects which pass programmable threshold conditions on transverse energy are sent to the CTP . Types and coordinates of identified objects are also sent as Regions of Interest (RoIs) to the second-level trigger system (LVL2) [2]. In order to achieve the required latency of 2μs the trigger is implemented as a system of purpose-built hardware processors. The Multi-Chip Module is the key component of the Pre-Processor system. It holds the PPrASIC chip, where the main data processing functions are implemented.

The testing procedure as well as large scale production of the MCMs will be described in this note. Section II gives an overview of the Pre-processor system as a whole. The Multi-Chip Module functionality and production technique are described in the Section III. The test-setup and test procedures are presented in the Section IV. Finally Section V gives a description of the PPrASIC wafer production and the production cycle of the MCM.

II. The Pre-Processor System

The Pre-Processor System performs complex processing of the analog trigger tower signals, which are received from the electromagnetic and hadronic calorimeters. After reception of differential analog signals, Analog Input boards (An-In) of the

Pre-Processor convert them into unipolar signals and adjust a zero baseline for each input signal.

The rest of the signal processing takes place in the MCM and will be described in the following section. The data processing in the Pre-Processor is done at rate of 40 MHz with a maximum latency of 15 clock cycles (375ns)[3]. As a result the Pre-Processor generates three digital streams, containing the transverse energy deposits with the corresponding bunch-crossing. These data are serialized and distributed via LVDS links at 400Mbit/s to the CP and JEP subsystems. In addition the Pre-Processor provides a readout stream for system diagnostics. The digitized raw data and pre-processed results are sent to the Data Acquisition system (DAQ) as soon as an event has been accepted by the Level-1 Trigger.

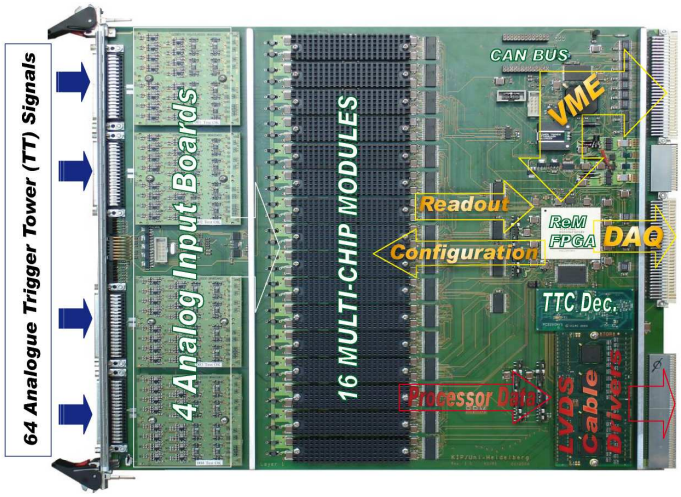

Figure 1: The Pre-Processor Module

The complete Pre-Processor system consists of 8 crates. Each crate contains 16 Pre-Processor Modules (PPMs). The 64-channel PPM is realized as a 9U VME Printed Circuit Board (Figure 1). Each PPM carries 16 MCMs and 7 daughter cards. The 4 An-In boards adjust the analog input signal, before digital processing by MCMs. After digital processing signals are sent to the LVDS Cable Driver (LCD) card where they are routed and fanned out before transmission to the subsequent subsystems. The readout is done by means of Rear G-Link Transmission Module (RGTM), which send the readout data to the ReadOut Driver (ROD) . Temperatures of all units on PPM, as well as board internal supply-voltages are read out by a CAN-controller. The entire data space of the module is accessible through VME.

III. The Multi-Chip-Module

Almost all signal processing tasks of the PPM are performed inside the MCM. Each MCM processes four trigger signals.

A. *MCM functionality*

MCM is designed as a compact module, which holds 9 components in non-packaged form . A fully assembled MCM without lid is shown in Figure 2.

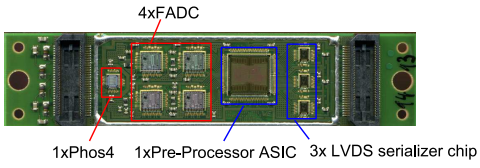

Figure 2: The Multi-Chip Module

The chips on the MCM and their corresponding tasks can be summarized as follows:

- Four Flash ADCs (AD9042, Analog Devices)
  - these FADCs digitize the input signals with 10-bit resolution and a sampling frequency of 40 MHz;
- Timing chip (PHOS4, CERN Microelectronics Group)
  - the Phos4 delays the FADC clock with respect to the system clock in steps of 1 ns within a LHC clock cycle;
- Pre-Processor ASIC (PPrASIC)
  - Each PPrASIC processes four digital channels and provides readout. Further tasks are: real-time bunch-crossing identification, channel synchronization, final transverse-energy calibration, pedestal subtraction, pre-summing of jet elements, bunch-crossing multiplexing, serial data transmission;
- Three LVDS serializer chips (DS92-LV1021, National Semiconductor)
  - The LVDS serializer chips transmit the processed data to the subsequent processors at a rate of 400 Mbits/s;

A simplified block diagram for the processing of one channel is depicted in Figure 3.

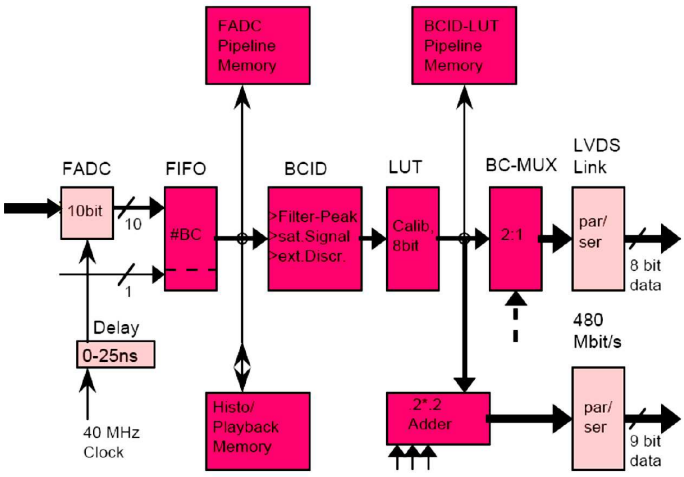

Figure 3: Block diagram for the processing of one calorimeter channel on the MCM

The dark functional blocks are integrated on the PPrASIC, whereas the shaded blocks live on other chips of the MCM. The incoming analog signals are digitized with 10-bit resolution at a sampling frequency of 40 MHz by the FADC. The digitized data are latched into the PPrASIC, which performs all digital processing. The PPrASIC generates three real-time streams of data, which are serialized by the LVDS serializers. 10-bit LVDS data words are sent to the CP and JEP systems. The CP receives two data streams containing multiplexed energy values from four channels. The third stream to JEP contains the energy sums of these four channels. These pre-sums form the jet elements for the JEP. Two serial interfaces provide the readout of raw FADC data as well as all energy values resulting from the BCID algorithms and Look-Up-Table (LUT) calibration. The data can be read out upon each Level-1 Accept. Additional data produced by histogramming and rate-metering blocks in the PPrASIC, come within the readout stream but independently of a trigger decision. These data can be useful for monitoring of trigger and calorimeter performance studies. The detailed description of the MCM and PPrASIC tasks can be found in [6].

B. MCM production technique

The base of the MCM is a multilayer high-density printed circuit board (PCB) with microvias for layer-to-layer contact. The PCB has 4 copper layers, 2 epoxide Prepreg layer and 1 FR4 layer. The copper layers of the PCB are interleaved with Prepreg layers and FR4 core in the center. FR4 material is made of epoxy resin that saturates woven fiberglass. The required micro vias are formed by laser drilling. The combination of this semi-flexible PCB sticking to a 0,8 mm copper plate - to realize an effective heatflow - is manufactured by Würth Elektronik company [8] . This technology is listed by the brand name TWINFLEX®.

All "foot-prints" of dice on the substrate contain a copper-area, covered by a thin gold layer in the center. These areas are studded with so-called "thermal vias" (no electrical function), whose purpose is solely the conduction of dissipated heat to the copper-plate. All nine dice are placed and fixed using heat-conducting glue. A wire-bonding machine connects the pads on the dice to the pads on the substrate. After bonding is done, the "glob-top" coverage is applied to the vulnerable components on the MCM to protect them from environmental, mechanical and electrical damage. The MCM substrate is covered by a brass-lid; it is soldered onto a copper-frame in the top-layer and serves as a electro-magnetic shield against imposed noise from hostile surroundings. And finally a metal body made of studded metal (with enlarged surface) is glued to the copper-plate to provide exchange of dissipated heat with the surrounding air-flow in the electronics crates[7].

Components such as capacitors and resistors are connected to the multi-layer structure using surface-mount technology (SMT). On each end a 60 pin SMD connector from SAMTEC (BTH030) connects the MCM to the Pre-Processor Module[3].

IV. Production tests

Being a complex electronic device, the MCM needs to be thoroughly tested. The MCM test-setup is shown in Figure 4.

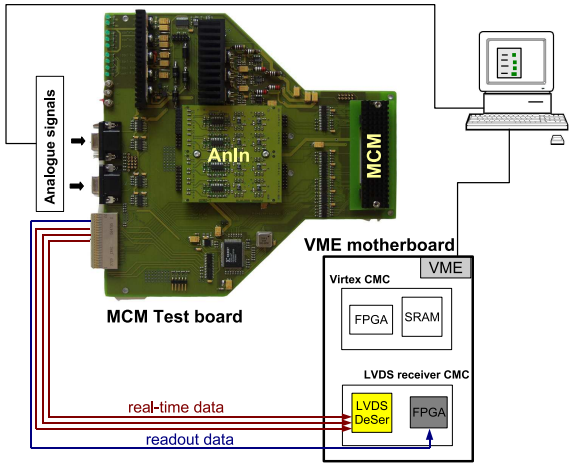

Figure 4: MCM test-setup

A. Test environment

The test environment has VME-infrastructure, which provides computer-controlled input generation and output capture. It consists of:

- a VME crate with a general purpose motherboard containing two daughter boards: LVDS receiver Common Mezzanine Card (CMC) and Virtex CMC,
- a specially developed MCM Test Board,
- a standard graphics card used as analog signal generator ,
- a computer, on which the test software is running.

The main block of the test setup is the MCM Test Board. It emulates the MCM environment on the PPM and holds two components of the final Pre-Processor Module: an Analog Input Board and the MCM to be tested.

The signal generator is programmed to generate the expected pulse shapes, "typical signals" obtained from test-beam studies and special test vectors. The analog output from the signal generator is sent to the analog input of the Test Board. After transformation is done on the An-In board, the incoming analog signal propagates to the MCM for further processing. The output of the real-time path is received by the LVDS receiver Common Mezzanine Card (CMC). The data of the readout path are received by a Xilinx FPGA, on the same CMC card. The data received by the LVDS receiver CMC are transmitted to the Virtex CMC card, which hosts a large SRAM buffering the data of the real-time path. Finally the data from both, the real-time and the readout path, are sent via FPGA on the motherboard to a Dual Ported RAM (DPRAM). This memory is read out by VME and thus data are transmitted to a computer, where they are analyzed.

B. Tests and Test software

A multitude of separate tests were combined in specially developed software for the production tests.The tasks of the test

software are: a complete test of all functions of PPrASIC and MCM in automatic mode, a detection of nonfunctional blocks on the MCM, a provision of a test environment for further investigation of the faulty MCMs. The last two functions are required for the repair cycle, where the faulty chips have to be identified and replaced.

The test software consists of three main packages: the configuration package, the analog handler, the test handler.The first package is responsible for register settings used in the tests, the second package contains the pulse library and generates the analog test vectors, the third package configures and runs the tests. The sources of input data can be two-fold: analog or digital. The analog test patterns are used mainly to test the FADCs, BCID algorithms, and histogramming built into the PPrASIC. The digital patterns - pre-loaded in PPrASIC playback memory - serve to test the digital part of the MCM.The readout and real-time data captured in the memories are compared to each other and to the precalculated expectations. Tests of certain functional MCM blocks with both analog and digital input, allows to determine with high precision any malfunctioning blocks.

During production tests the software can be used in two main testing modes: PPrASIC Wafer test or MCM test. In the Wafer test mode only PPrASIC functional blocks are tested. In addition, the software controls wafer-probe station manipulations, namely stepping from die to die. The single Wafer test takes 1 minute per die; testing a whole wafer in one go needs 5 hours. In the MCM test mode all dice on one MCM are successively tested. This takes 2.5 minutes per MCM.

The test software was written in the C++ language using Qt libraries. A graphical user interface provides a test menu-guide for the user.

V. MCM LARGE SCALE PRODUCTION

The MCM large scale production consists of two major stages: component dice production and assembly of the MCM. At the first stage all components produced have to be tested before being placed on the MCM substrate. This allows elimination of the faulty dice at the first production stage. At the second stage, the complete MCM-assembly is done in several steps with intermediate testing of the MCM functionality. This strategy allows to detect faulty components and assembly failures at early stages of the production, thereby improving the initial production yield.

A. PPrASIC wafer tests

Among the chips on the MCM, the Pre-Processor ASIC is the major component as it performs the ATLAS-specific digital data processing for four trigger towers. The PPrASIC is a custom-designed chip, designed at KIP and fabricated by AMS (Austria Micro Systems). The physical properties of the PPrASIC are briefly summarized as follows:

- The size of a the PPrASIC is 8.370 * 8.375 mm^2.
- The design is realized as a "CUA 0.6 μm" process.
- Each PPrASIC contains logic and memories covering four signal-channels (950 000 transistors equivalent).
- The number of PPrASICs per wafer 192.
- The total Memory per PPrASIC is 8.125 KByte.

Each PPrASIC die is subject to a full functional test before placement on the MCM substrate. The PPrASIC wafers were tested in the KIP "clean-room" using test-hardware and the wafer-probe station to facilitate stepping from die to die(see Figure 5).

Figure 5: The PPrASIC test-hardware mounted in the wafer-probe station.

The test set-up for the wafer test is similar to the set-up described in Section IV, with some modifications on the MCM side. For the wafer tests the MCM Test board carries a "Needle Card" connected via adapter to an MCM-substrate with missing PPrASIC. The "Needle Card" has the pins to contact all the pads on the PPrASIC die on the wafer. For each wafer undergoing the test procedure, a wafer map is generated(see Figure 6). It contains the test results for each single die using an 8-bit color code. Those dice that passed the test are marked as "Known Good Dice" (KGD) . Later at a company, wafers are cut to individual dice, from which all identified KGD are selected and available for further use.

53 wafers with 10176 PPrASIC dice were produced and tested. Out of this number 4306 dice were found to be KGDs, giving a yield of 42%.

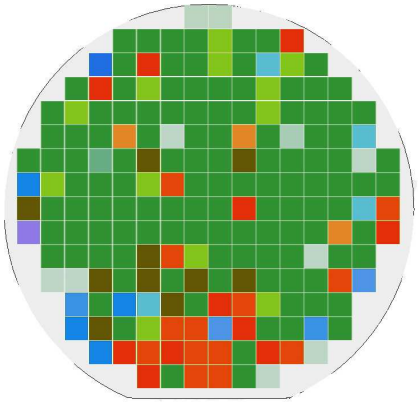

Figure 6: Wafer-maps showing test-results using an 8-bit color-code

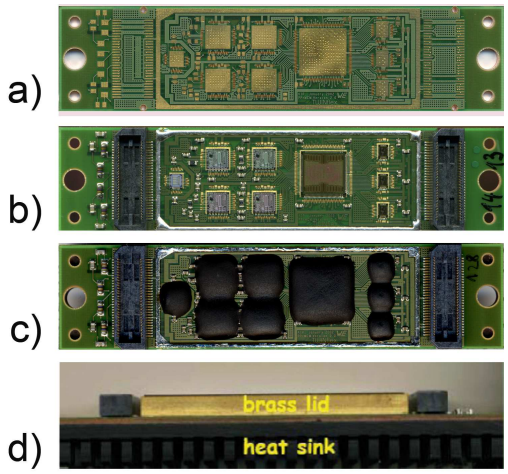

Figure 7: MCM assembly steps: a) MCM substrate; b) MCM with all dice bonded on substrate; c) MCM with glob-topped dice; d) MCM with brass and heat sink (side view).

B. Production Cycle

As the MCM was fully designed and developed at KIP, the first few modules were produced at KIP. Such in-house MCM production helped to understand the production problems and to develop strategies for the large scale MCM production.

The rest of the MCM production was done by industry. The MCM substrates were produced by WÜRTH Elektronik, while mounting of dice and SMD components, wire-bonding, and encapsulation was done by Hasec[9]. Figure 7 shows the MCM assembly at different production steps. Those were:

- production of 4-layer FR4 substrate backed by a 0.8mm copper plate by WÜRTH,
- **electrical test of the routing-tracks**,
- **bonding test by HASEC,**
- passive components soldering applying SMT technology,
- chip mounting,
- ultrasonic wire-bonding,
- **MCM Quality Assurance tests at KIP** ,
- application of glob-top over the 9 active chips,
- encapsulation of MCM hermetic brass lid; gluing of a heat sink for dissipated heat exchange,
- **MCM Quality Assurance tests at KIP**.

C. Production Results

At the time of writing the MCM production is fully accomplished. The number of functioning MCMs is 3012; the number of MCMs, which were found faulty during the production is 776. All test results as well as supplementary information for each single MCM are stored in the database, which is accessible via WWW.

After further investigations all faulty MCMs for which non-working chips could be determined, undergo a repair cycle at the mounting company. Different kinds of failures (short-circuits, faulty chips, bond faults etc.) make the investigation process rather complicated. In cases where the software alone is not sufficient to find the problem, a complex analysis using a microscope, an infrared camera and an oscilloscope is used.

VI. Conclusion

More than 3000 fully functioning MCMs are produced and ready to be installed in the ATLAS Level-1 Calorimeter Trigger. Thorough tests during the large scale production of the MCMs show an overall MCM yield of 80%. The experience gained from the large scale production of the MCM is reported including the optimization of the test procedures, observed problems and corresponding solutions.

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