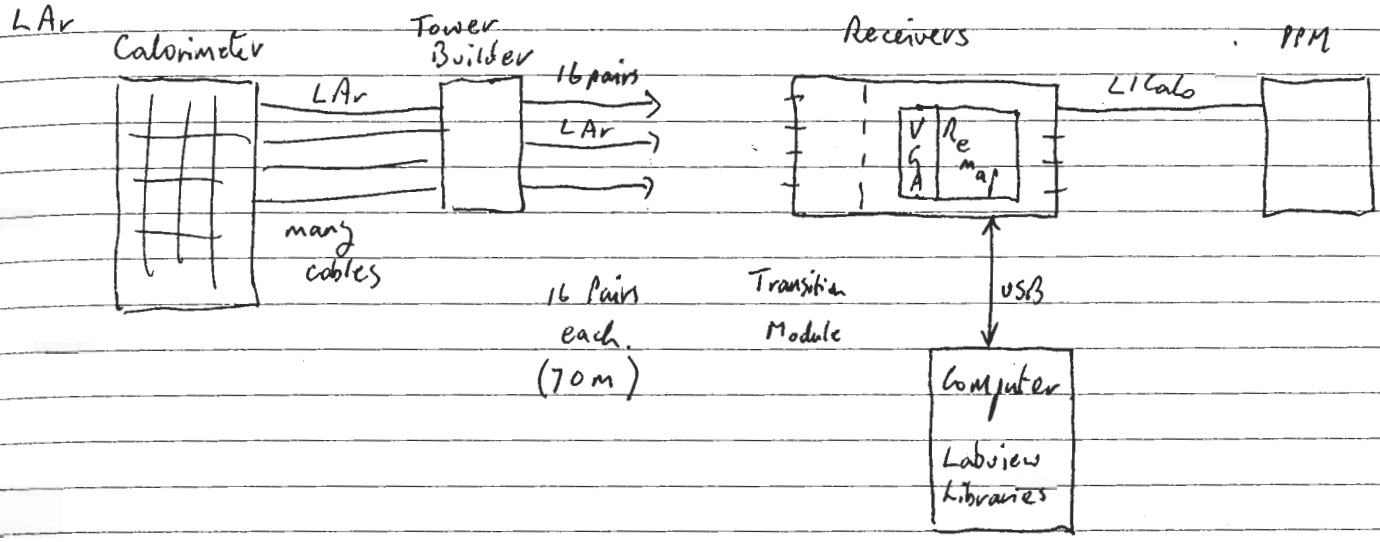
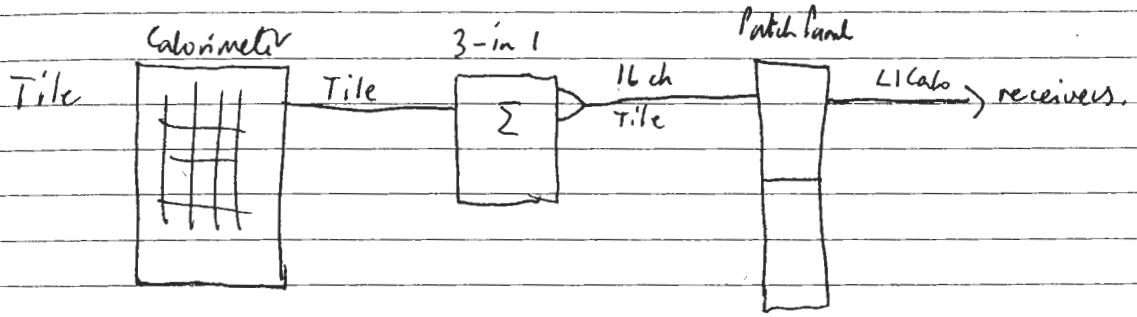
3-Aug-2004. Pilot Installation





Wireless Network Key for AirTgeCern: Qubeley Bygzam

Tile Calo Web at Cern:

Test Beam Meeting 15:30

Martin Aleksa CERN.
Paulo da Silva

Run at $\theta = 1.0$ π, e high eng, e lower energy.
$\theta = 1.1$
$\theta = 0.8$

e^- at 50 + 100 GeV.
+ 180.

Wednesday 4 - Aug - 2004

Computers in the test beam:

pctb-lv1c-ros ϕ1 . atlas.cern.ch
~~pctb-lv1c-ros ϕ1~~
cctb - lv1c ϕ1 172.29.120.101
ϕ2 .102
ϕ3 .103

Wireless TAC or

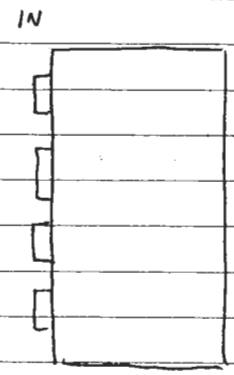
ssh lxcalo_daq@pctb atlgw.cern.ch from lxplus

This actually connects to "pcthserv". Then can ssh to

SSHStarter needs HOME and DISPLAY
H:\ HEPNT132.pp.rl.ac.uk

Attenuation cut SICHF each!

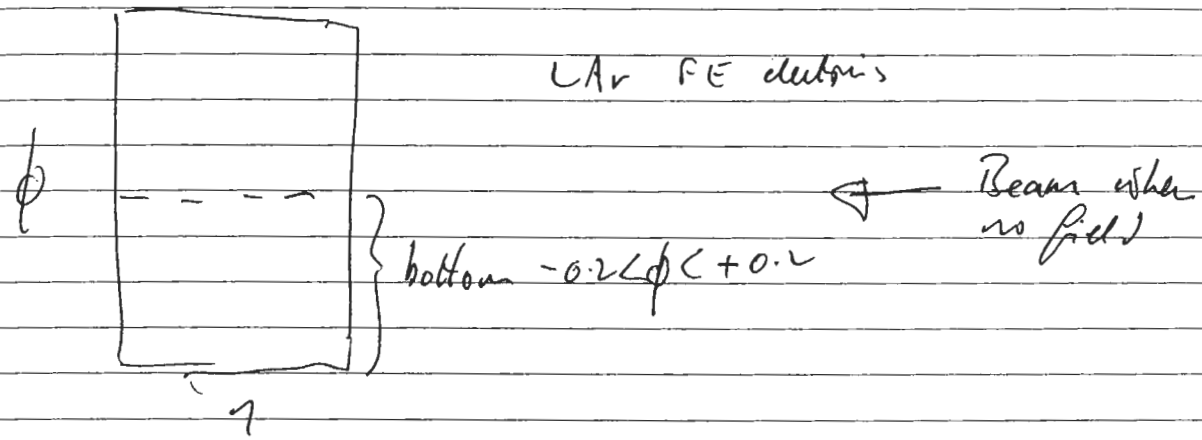
Connection of outputs from PPMs - thoughts.



Each of the 4 inputs takes 1 cable, with 9 active signals.
The most efficient pinning would be 9 consecutive channels, using 2¼ MCMs. = 3 MCMs. This would produce 5 BCMuxed signals, 3 LVDS wafers, so 2 cable bundles (1 bundle = 2 ~~cables~~ wafers).
For 3 input cables, ~~&~~ 6 bundles for CPM.
The least efficient
For Jet, 9 part jet elements. 1 cable bundle takes 4, so need 1 per input per ~~an~~ input cable

So for 1 cable 6 bundles to CPM + 3 to Jem = 9.
overall need 18 bundles.

Cable existing: MD ~ 10 bundles
UK ~ 20+



14 FE boards per Tower Builder

16 cell in ϕ x 56 in η in Middle Layer. These are the point at which LAr direct the beams - the middle layer captures most of the energy.

Weekly Meeting.
Integration Status.

Pixel	ready to try with DAQ.
SCT	Computer + ROD Problem.
TRT	Naming Problem,
MDT / RPC	Integrated.
LAr / Tile	Timing Studies ← Looks to see cable signals.
LI	Rod Busy coming into use
LICalo.	

180 GeV	40% e^- in electron beam,	Momentum is known to ~1%.
150	1% e^-	
100	30% e^-	
50	75%	
20	15% in π beam (not e^- beam)	

Calorimetry know that combined data run makes sense. Not clear if muon dets get known how to do this.

Total of 6 LTPs. ID, Tile, LAr, Muon, LICalo, LIMuon

CTP Land: 104 - by R. Spiwoks.

CTP-OUT has only 5 outputs for 6 LTPs.

Testbeam computing setup

Wireless : tgc, muon : inside firewall
air tgc cern : outside firewall – needs key, see p1.

Access from outside.
- ssh to lxplus
- ssh l1calo-daq @ pctbatlgw.cern.ch

This takes you to the test beam server pctbsrv (RedHat 9) which should not be used for work

From here ssh to any other test beam machine:

pctb-lvlc-ros01 : our ROS PC

ctb-lvlc02 : will be PP crate
ctb-lvlc03 : ROD/TTC crate
ctb-lvlc04 : CP/JEP crate.

Default shell is tcsh. Type bash to get usual L1Calo development setup.

1500 Testbeam Meeting (Benjamin et al)

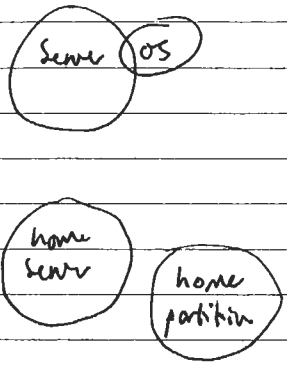
- Beam 1 hour since midnight, then since lunchtime.
  - Pixel DAQ removed - f. invalid events.
  - TRT - VME off means auto zero supp; Bytestream converter fail online.

Want to get back to Pixel + TRT together.

- Analysis problems with Athena: No online monitoring

Muons OK
Tilecal OK.

Event Filter - Driver problem prevents use of 2nd CPU on dual-CPU machines.
Server Problem - big overnight change to separate servers from logins.
Previous home file system was served with wrong protocol. Corrected.



3 machines.

AFS CVS update doesn't work, even over SSH.

3 Programs: Ruby, Day, # scan.

Prio to Monitoring. 1530 - 1800
TRT 18 - 20
Saclay - Tom Muller 20 - 22
DAQ 22 →

CVS only via SSH.

LI Calo Mtg

Analy cables. 2 10m + rst are 20 to connect receiver to det.
Trg pp from patch to receiver.

LAr are 70m, Tile are 60m (+ extra).

Receiv have Type 1 boards.
No control on the gains. Need laptop running labview.

PPr: SRAM is OK. Control of Asic is OK.
Still timing problem on Asic readout. (same as event readout),
S-link to ROD - 40 MHz crystal direct to S-link.
+ serial termination.

2 PPMs, 1 LCD all routed (not swapped) 30 MCM (at least 1 bad ADC).
2 RGTM electrical.
All 8 Ains

Computing - concurrent boots.

Want to study FADC's.

CPM Alive.

JEM Configure from Flash OK.

CMMs 2. Both have Esum up-to-date.
RH has up-to-date cf
LH has jet up-to-date. / cf a bit out of date.

RODs/ROD. 4 RODs mostly connected. S-links have come up.

TTC ready to go. Clock cabled, but not centrally.
Busy cabled.

S10/DSS config.

Online/Databases. All s/w built, late patches added.
VME h/w byteswapping. DF 10, Online 22.

We've always used bash. They use tcsh. Must type bash.
Run pkg-dg under tcsh.

CVS - there's no AFS, so use SSH.

Histo I am Sam
Hal Sam

Programm (a) Test PPM
(b) Rot of System
} Parallel

Computing setup

6 Sep 2024

Access from outside (only via lxplus)

- ssh l1calo-daq@pcthatlgw (detector_2024)
  → server machine, don't use this
  from here, ssh to our machines.
  then type 'bash'

Computers and crates

pctb-l1c-ros01 = our ROS PC

pctb-l1c-onl02 = our desktop PC.

cttb-l1c02 : ROD crate, : l1c02-cprod0 : PPM DAQ, 0x500
cprod1 CPM DAQ
cprod2 JEM DAQ, ROIs
cprod3 Neutral (Rem.)

cttb-l1c03 : PPM crate. l1c03-ppm0
ppm1
tcm

cttb-l1c04 : CP/JEP crate l1c04-tcm
cmm0 : Energy, Readout 0x4
cmm1 : CP, Readout 0x9
cpm0 : slot 9
jem0 : slot 13

cttb-l1c06 : TTC crate l1c06-ttcvi
-dss0
-dss1

cttb-l1c05 : HD homebrew.

Databases

Test beam setup has special versions of:

~/.atlasrc
~/.bashrc

~/l1calo/scripts/setupcmt.sh (sets L1CALO_DB_PATH to /daqsoft area)

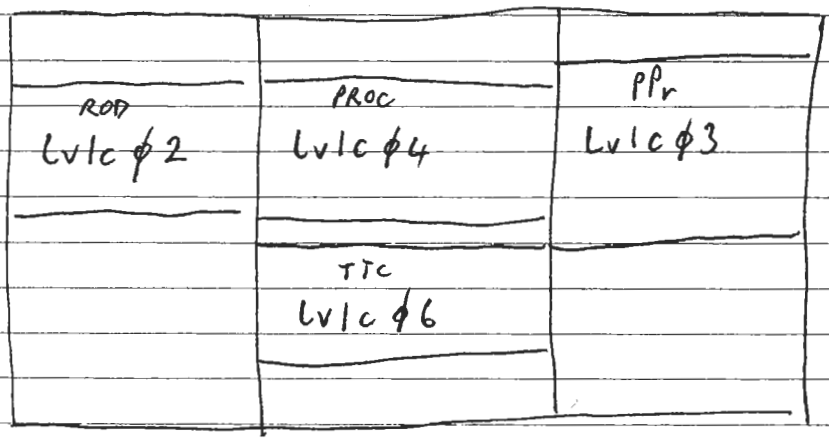
~/l1calo/dbfiles/dbfiles..../cmt/Makefile.requirements } install database files to /daqsoft area. (via link from installed).

Common database area:

(=v3)

/daqsoft/databases/current/L1Calo L1Calo specific

/combined ... for common partitions.



Weekly Meeting 8 - Sep - 2004.

- Dag overnight but not a lot. Some problems with beam settings.

- Timing - S2, S3 relative to master trigger is stable to ~ 0.5 nSec.
  TTC phase relative to master trig is recorded.

- There are low rate calibration triggers - rate ~ 1 Hz.
  [Tilecal Trig type will include info if its a calib trigger]

Detectors: Pixel - small problems with noisy links.
SCT - no new.
LAr - Trig tower studies still going on. Another 2 hours.
- Instability of reconstructed energy. Pedestal moves in run. temperature effects. avoid
Would like to Unload so that temperature stays high?
- Want to check coherent noise - short acq.
- SPACbus debug.

Tile - OK
MDT - OK
RPC - Problem.
Muons cosmics and gas regularly.

EF - crashing and also breaking LVL2.

Beam. + 180 GeV
η scan, energy scan

15 - 18/9	- 250 GeV	⇐ Target to end debugging.
18 - 19	- 20 GeV	
20 - 21	- 10 GeV	
22 - 29	- 1 - 9 GeV	
29 - 5/10	- 250 GeV	— Including some debugging time
5 - 12/10	25 nSec	
13 - 19/10	1 - 9 GeV.	

Need magnet to move beam into tower builder.

offline. Refit in electronic log of LAr

- Can't start HDMC with concurrent.
- Without Hanebrew, PPM turns off.
- Without TCM, all seem to work.

Tem links come up; cPM DAQ links work. cPM Rol does not

cPM (I will look with electrical, neither with optical, PPM not seen.

PPM Measurements. - Power Supply.

- No dip in 5v (tm) at 4.7v)

- 3.3v on backplane. Dips to 2.5v for 65 μsec

With concurrent removed, dip is down to about 3.0v
which is above PPM current threshold

Xavier de la BROISE labroise@cea.Fr
Alain LE COGUIE lecoguie@cea.Fr

1. Crate. Send from MD.
   Check specs for concurrent.
   Tag them Eric to check specs.
   Remove MCMs in unused channels.

2. One PPM goes back to MD.
   3rd PPM doesn't have DC-DC converter. Hans will.

3. MCMs.
   Read & test MCMs.
   14 return to MD, 16 stay here.

4. Readout Asic → FPGA.

Power Fluctuation with Hanebrew: 3.2 down to by 320mV
duration 30 μsec

Daij. Thome is not backed up but again more stable.

PPM Front Panel

⊙	·	Rem FPGA (Green OK, Red error)
⊙	·	LCD CP Drive
⊙	·	LCD JEP Drive

Power OK	⊙	· Not Used
~~Daughter~~ Board Sel ~~Mezzanine~~	⊙	· Not Used
~~VME Status~~ = TTC Status 1	⊙	· Not Used
TTC Status 2	⊙	· Not Used.

↑ Expected Lights shown ⊙

Glink Rx modification on ROD DB

Channel	Component	Pin
A	U10	13
B	U11	13
C	U10	1
D	U11	1

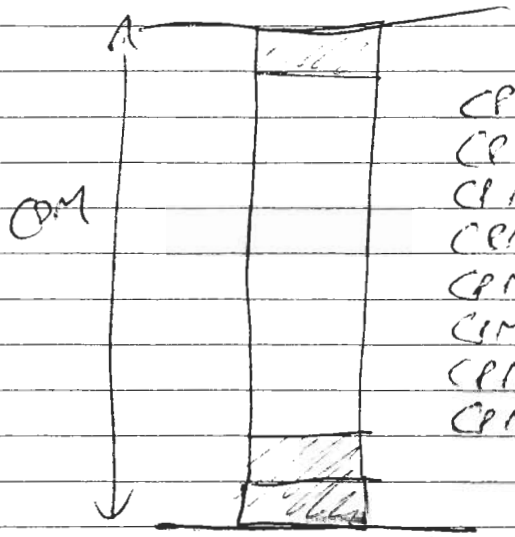
Channel D for ROD CPM DAQ 1 changed Mod. ID #6
Channel B and D for ROD CMM 3 changed Mod. ID #8

12TH SEPTEMBER

LVDS CABLING :- WE WANT :

CPM	EM	A				
CPM	EM	B	TO			
CPM	EM	C	..	JEM	EM AB	TO
CPM	EM	D	..	JEM	EM CD	..
						..
CPM	HAD	A		JEM	HAD AB	
CPM	HAD	B	..	JEM	HAD CD	..
CPM	HAD	C				
CPM	HAD	D				
↑ LOGICAL NAME			↑ ACTUAL CABLE	↑ LOGICAL NAME		↑ ACTUAL CABLE

LVDS CABLES AT CPM RCD
(SEE ~~2a~~ FIGURE 16 IN PPM SPEC)



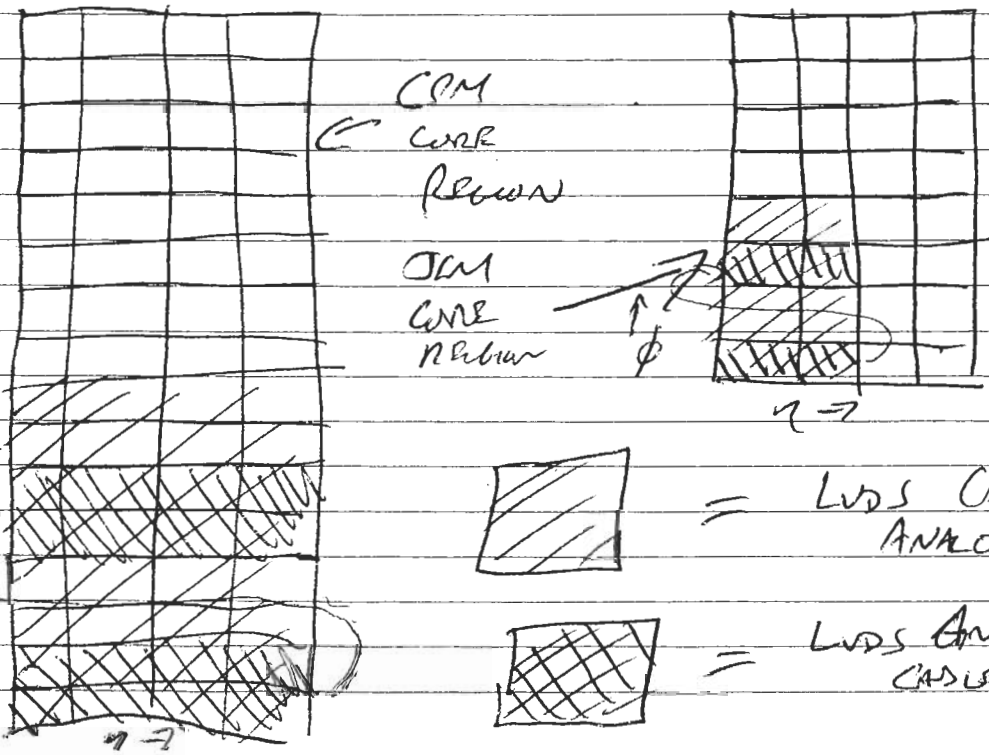
CPM EM A
CPM EM B
CPM EM C
CPM EM D
CPM ~~EM~~ HAD A
CPM HAD B
CPM HAD C
CPM HAD D

→ GO TO OBVIOUS PLACES IN CPM

JEM EM AB
JEM EM CD
JEM HAD AB
JEM HAD CD

→ GO TO LEFT HAND (LOW ETA) INPUTS IN JEM

WHAT THIS MEANS FOR CPM AND JEM:-



= LVDS CABLED, NO ANALOGUE INPUT (OR MCM)

= LVDS AND ANALOGUE CABLED (WITH MCMs)

DAC values for chan C/D of MCM 2.

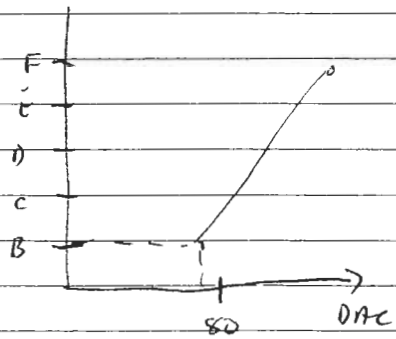
DAC_{10}	$LVDS_{10}$
128	123
2	262_{10}

Beam is 0.55 100 and so for e and $\bar{e}$.
Then 0.65 " "

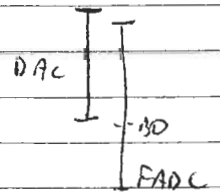
DAC Values in MCM 1, Chan 4 with DAC.

DAC		MDMC	
FF	Freezes digital value from ADC at	3FF	2.254 V
Cϕ	ADC Pedestal + noise	3E6, 2E5	2.104 V
80	" "	3B7	1.95 V
40	Pedestal only	Bϕ	1.8 V
60	" "		
70	" "		
78	Ped + noise		
74	Ped + little noise.		

So don't understand (a) why minimum is Bϕ
(b) why limit is so high it freezes at ~ E6 for DAC



So looks like



MCM 2, Chan A. Constant value ~~width of DAC setting~~ ~~0004 Bϕ~~ 3ϕC
from DAC ϕ to

0	constant ~~BAC~~ ~~BAC~~ 00C	~~0004~~	0C'0' = 30
80			
AQ	2ϕE ~~BAC~~ constant	~~0004~~	~~0004~~ 0E'2' 3A
Bϕ	00F	~~0004~~	0F'0' 3C
Cϕ	30F		0F'3' 3F
Eϕ	211 + noise 110		11'2' 46
Fϕ	012 no noise		12'0' 48
Dϕ	110		10'1' 41

This notation mean just 2 bit in the nibble

Still MCM2 chan A.

DAC $\phi 0$ = 1.65 V
FF 2.246 V Correct. Dynamic rage 600mV.

Homebrew Xilinx Initialisation Instructions.

ssh heidelberg@ecctb-lvleϕ5
dbhdmc
load database for this computer
Sel PPM-FKA from PPMϕ (which is PPM1 elsewhere)
LOAD
directory ~~/home/~~ L1calo/ppmSeries/.../firmware/xcv1000e.bit
(for reconfpga)
lcd_cp.bit
lcd_jp.bit

Then load. Observe green lights

There is also a 'ppmwatch' program on homebrew

Decide to power down and on again.
- Start Run Control.
- Loaded Xilinx
- Check no replay mode in MCM1 all channels.
- Bypass BCMux in chan A/D.
- Load chan D with 60 — Observe same FADC values as before (60).

∴ Reboot / power down has not helped

13-Sep-2004.

Trying to time calorimeter relative to Beam.

LAr tripped off and no-one knew yet not main run.
Can't tell when a run is underway or not.

Beam vertically out of Calo.

3-o clock Meeting.

Muctpi is integrated.
3 cavity shots 8 - 4 - midnight. ~15 minutes.

Wednesday functional test start/stop repeated. MD 8-16.

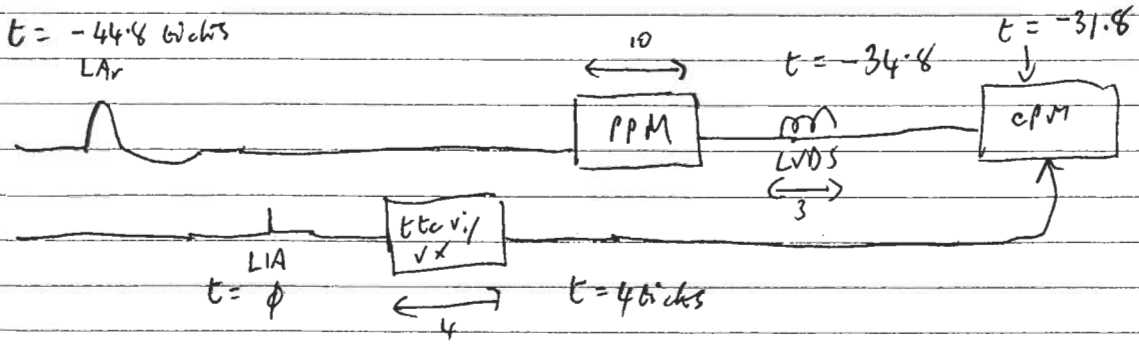
Tilecal Voltage problem on Sunday.
Problem with 15 with lots of history. 76731

Delay - Peak of tilecal pulse (π) to leading edge of LIA = 1.12 μsec
LAr pulse 1.17 μsec

Ros/DFM/SFI Day expert: Louis Tremblet + Alina 71204.

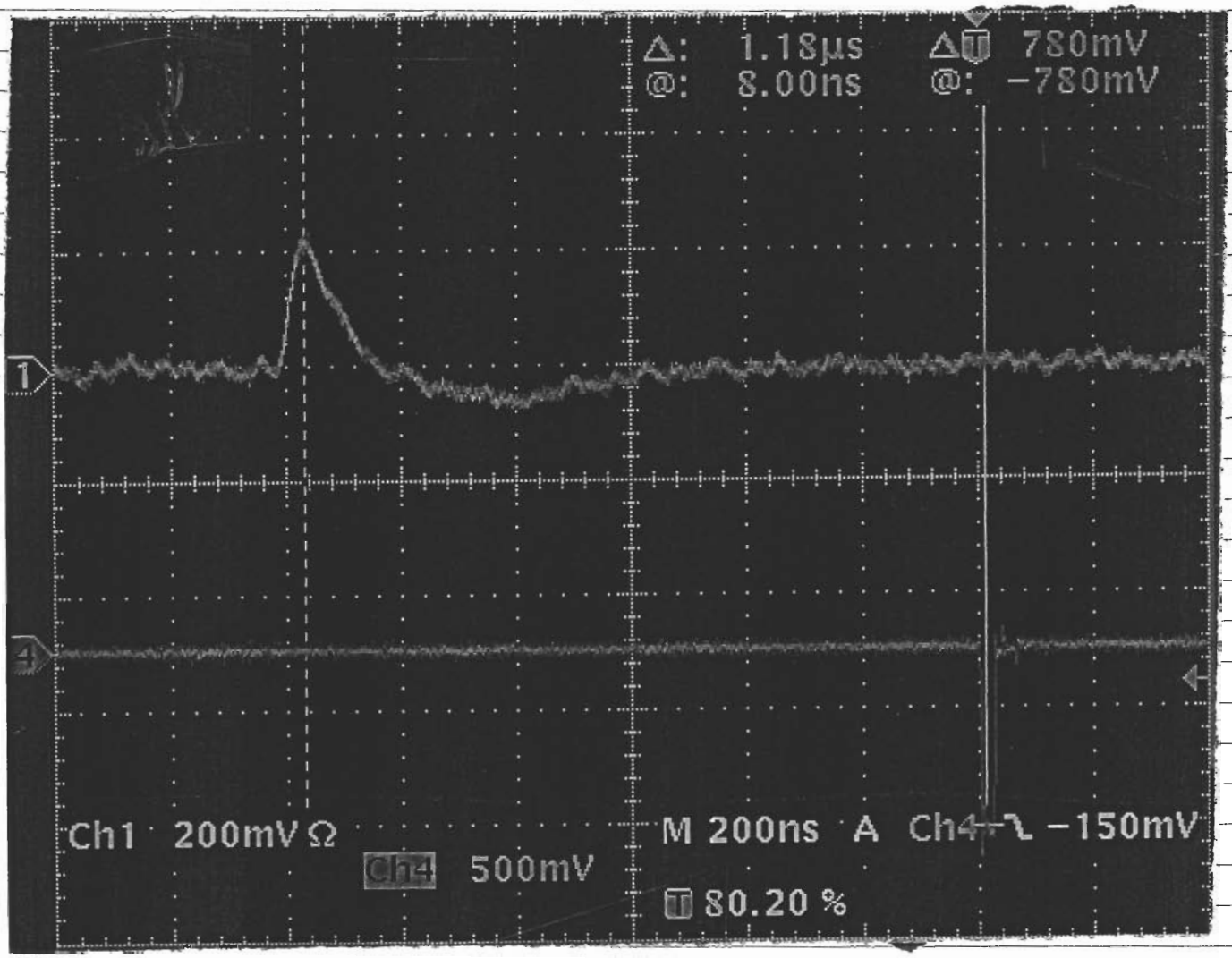
Tilecal is 1.12 μsec = 44.8 clocks
LAr 1.17 μsec = 46.8 clocks
] before LIA.

Plan: Add 2 ticks to LAr to bring them in time.

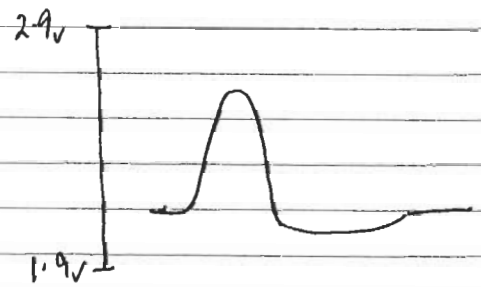


offset to readout should be 34
readout from 34 - 38

LAr



Note on DAC and FADC offsets. Absolute voltages at FADC input:



DAC: 1.7 to 2.15v (≈ 500mV range) 8 bits, 2mV/count.

FADC: 10 bits obtained from 12. 10-bit ⇒ 1mV/count

14/9/04 Now at 20 GeV π (was 180 GeV yesterday).

Timing now: Tile Δ (LIA − pulse pk.) = 1.15 ns
leading edge
−1.16 ns
(diff cable lengths)

1500h Meeting.

cerenkov counter problem - access this am.
Low-en π with some e⁻ (lead absorber).

TRT stand-alone request for 2 hours.
SCT ROD F/W problem.
MUCTPI out.

Programme: 17:00 –
Today 0.35, 0.65, 1, 0, 20 GeV. each takes 1 hour. Ending Midnight.

φ displacement − 0.2, etc η scan e⁻ whole night.

Programme:
16:00 Wed − 250 GeV.
Mar 20 20 GeV.
21 −10
Wed 22 MD. then VLE (1–9). } η < 0.8.

29–3 Oct η > 0.8., −250 GeV.

12–19 Oct 1–9 GeV.

Tilecal remains till 22 Nov. (earlier was planned).

- Jem & CPM readout is OK.
- Have zeros
- Tile calib path is at same time as real path. } Tile.
- Mati, LIA with real calib path.

Our 4pm meeting.

Priorities:

1. Find timing window for readout using histos. cPM
2. Set DAC to give FADC (8-bit scale) = 30. Set Link for offset of ~30.

1a In JEM, ← Find Pulses
└ Sort out two clear links.

3. Activate BcID; check timing in histos cPM and JEM
4. Activate BCMUX; Recheck histos - peak should be 1 tick later.

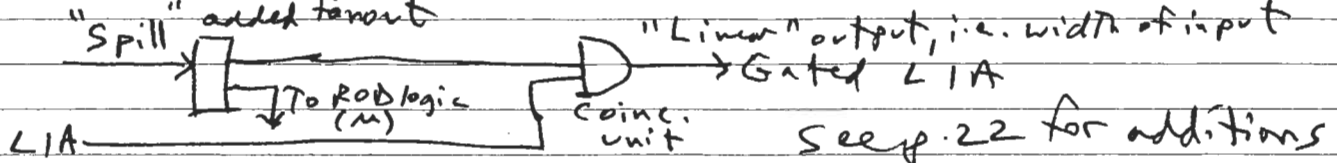
When second crate comes: work on readback of registers and mem.

Software: PPM config parameters: DAC, Phos4, FIFO for ADC, latch edge, LUT.

PPM DAC SETTINGS TO ACHIEVE COUNT OF 30

~~Acrate#~~		A	B	C	D
MCM #0	(0)				
MCM #1	(1)				
MCM #4	(4)	0XA4	0xA0	0xA5	0xA5
MCM #5	(5)	0xA7	0xAC	0xA8	0xA8
MCM #8	(8)				
MCM #9	(9)				
MCM #12	(12)				
MCM #13	(13)				

NIM logic used to gate L1A by spill:



See p. 22 for additions

~~To~~ PPM output to choose between A, B, C and D

B	A
C	D

$\phi \uparrow$, $\eta \rightarrow$

From HDMC Ppr SiF3_ channelAB:

A/D selected by 0/1

Ppr SiF3_ channelCD:

B/C selected by 0/1

EXPLICIT CURRENT CHANNEL MAPPING (15/9)

EM + HADRONIC ARE THE SAME (BAR 0.05 SHIFT IN PM1) (PLUS ADD 8 TO MCM NUMBER)

PPM MAPPING (EM)

	0-0.1	0.1→0.2
0-0.1	1C	1B
0.1-0.2	1D	1A
0.2-0.3	0C	0B
0.3-0.4	0D	0A
0.4-0.5	5C	5B
0.5-0.6	5D	5A
0.6-0.7	4C	4B
0.7-0.8	4D	4A

MCM num : Chan num

PPM (HAD)

0-0.1	0.1-0.2
9C	9B
9D	9A
8C	8B
8D	8A
13C	13B
13D	13A
12C	12B
12D	12A

CPM

0-0.1	0.1-0.2
3,1	3,0
2,1	2,0
1,1	1,0
0,1	0,0
3,5	3,4
2,5	2,4
1,5	1,4
0,5	0,4

CPM Location $\eta : \phi$ (0.3, 0.15)

JEM

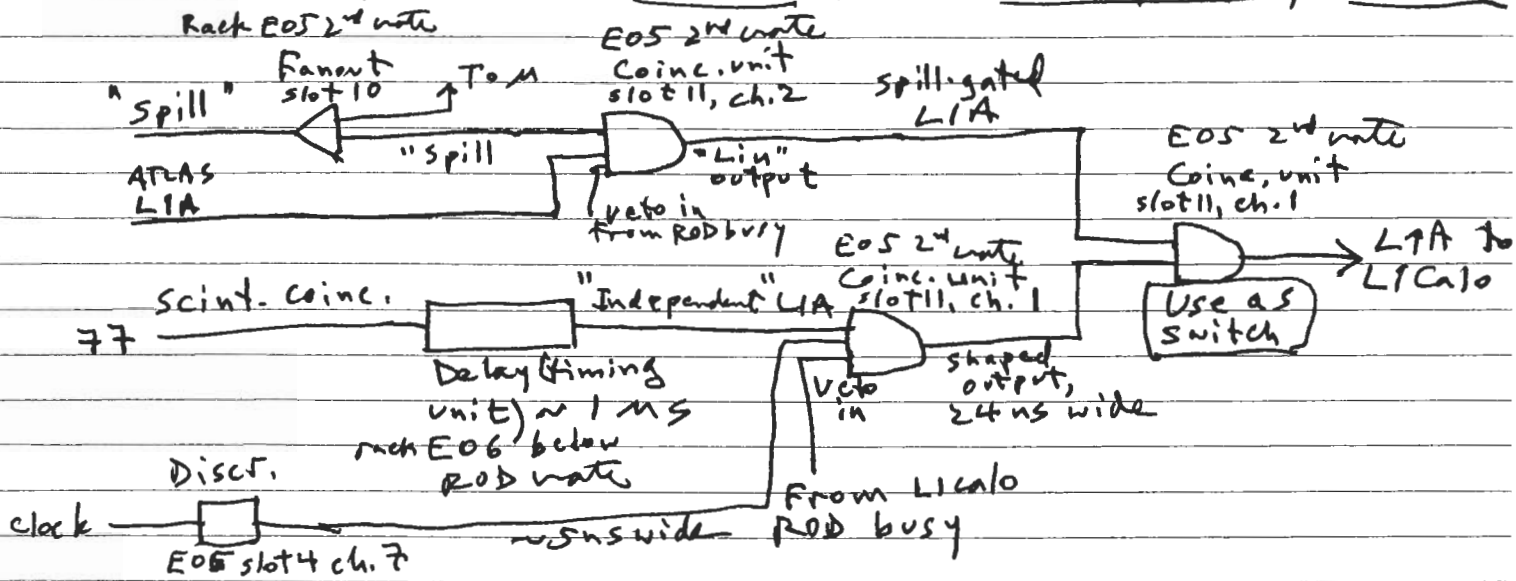
2,2
0,2
2,6
0,6

JEM Location $\eta : \phi$

I have extended the logic to allow us to try to run independent of the main L1A; so 2 options now:

(1) Normal L1A, but can be gated by a SPILL signal to avoid huge calibration signals. This was tested and works.

(2) Scintillator coincidence (upstream of calos) independent of main DAQ, to allow setting up without interruptions, etc. This needs beam to be set up fully & tested.



- Upper L1A signal is controlled by main testbeam DAQ. Can be gated by spill if both inputs are switched in. L1A pulse is correct width, so "linear" output (i.e. not reshaped) is used.
- Lower L1A signal is not gated by DAQ. Delay has not been set yet – use knob on timing unit to put it at the same time as upper L1A at input to coincidence unit. (i.e. leading edge.) NOT tested since no beam today!
- It is vetoed by our ROD busy – must check that this works ok.
- Output width is ~24 ns – must check this is ok.
- To make switching easy, I put both L1As into top 2nd channel of coinc. unit. Top switch selects spill-gated L1A, 2nd switch selects independent signal. DO NOT SELECT BOTH!
- Could put "independent" signal in coinc. with a clock, and set widths to only select signals at ~25 ns intervals if rate allows. I have not done this; it should be possible.

(Continued on p. 39)

15/9: 2 O'CLOCK MEETING

PROGRAM IS HIGH ETA (!) SCAN IN LAR.

HIGH ETA = 0.9 → 1.2 IF NO TRT SIGNALS

ALSO HAVE TO RELEASE REGIONS TO SEE THESE

ALSO 50, 100, 150 GEV TT'S LATER

HIGH ENERGIES 15/9 → 20/9 (20 → 250 GEV)

DO 20/9 → 21/9 20 GEV

THEN 10 GEV AND BELOW

RELEASED RECEIVER CARDS TO GAIN MORE ROOM FOR NEW ROM CRATE

AT THE SAME TIME, WE SWAPPED TO REMAPPING BOARD ID 16.

WILL RETAIL CONNECTIVITY LATER

LAR CABLES WITH 2 TOWER BUILDERS

ISAREC SHD CABLING UNS: 0.1 → 0.2 P0

0.0 → 0.1 P15

-0.1 → 0.0 P3

15/9: NEW CABLING REGIME

SEVERAL FACTORS HAVE CHANGED, INFLUENCING CABLING.

a) 2ND TOWER BUILDER

b) BEAM MOVED TO HIGH ETA (0.9 → 1.2)

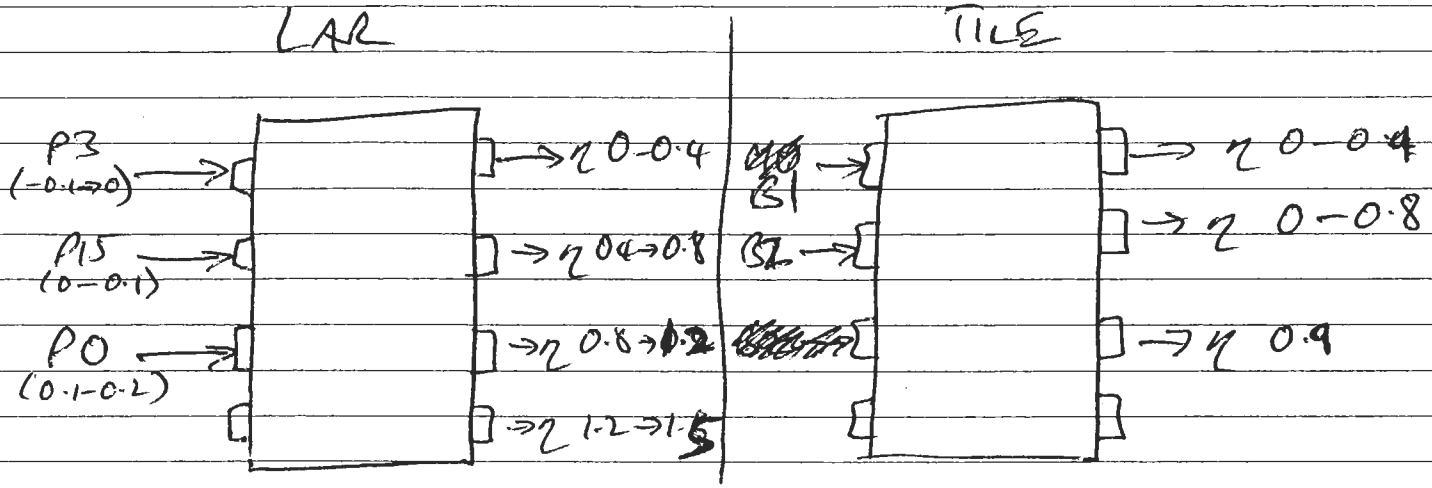
c) NEW REMAPPING BOARDS (16) PREFERED.

SO I'D BETTER DOCUMENT THE DETAILS

IF ISAGEN IS TO BE BELIEVED, LAR CABLES ARE NOW:

0.1 → 0.2	P0	TILES SEE	0.05 → 0.15 B2
0 → 0.1	P15		−0.05 – 0.05 B1
−0.1 → 0	P3		−0.15 → 0.05 M0

PROPOSAL FOR RX GATES



FOR LOW ETA BEAM, USE THE UPPER OUTPUTS OF THE RECEIVER

FOR HIGH ETA BEAM (NOW!), USE THE LOWER OUTPUTS CAR (NO SIGNAL FROM TILE)

SPECIFIC PIN REMAPPING REQUIRED (A LA FARDOULIS FIGURE 4)

LAR:

	0 / 0.1	0.1 / 0.2	0.2 / 0.3	0.3 / 0.4	0.4 / 0.5	0.5 / 0.6	0.6 / 0.7	0.7 / 0.8	0.8 / 0.9	0.9 / 1.0	1.0 / 1.1	1.1 / 1.2	1.2 / 1.3	1.3 / 1.4	1.4 / 1.5
−0.1 → 0	16	13	4	1	16	13	4	1	16	13	4	1	16	13	4
0 → 0.1	15	14	3	2	15	14	3	2	15	14	3	2	15	14	3
0.1 → 0.2	12	9	8	5	12	9	8	5	12	9	8	5	12	9	8
—															

RX OUTPUT A | RX OUTPUT B | RX OUTPUT C | RX OUTPUT D

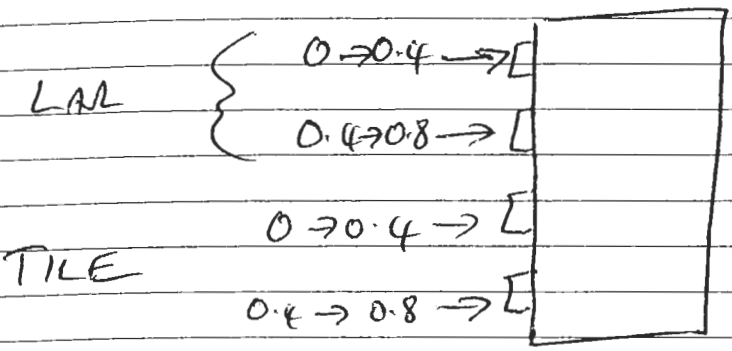
TILE:

	0 / 0.1	0.1 / 0.2	0.2 / 0.3	0.3 / 0.4	0.4 / 0.5	0.5 / 0.6	0.6 / 0.7	0.7 / 0.8	0.8 / 1.0
−0.05 → +0.05	16	13	4	1	16	13	4	1	16
+0.05 → 0.15	15	14	3	2	15	14	3	2	15
~~0.15 → 0.25~~	12	9	8	5	12	9	8	5	12

RX OUTPUT A | RX OUTPUT B | RX OUTPUT C

WHAT THIS MEANS FOR WHAT WE SEE IN PPM / CPM / JEM.

E.G. FOR A PPM CABLE LIKE THIS:—



PPM FM			PPM HAD			CPM			JEM		
0 → 0·1	0A	0B	1A	8A	8B	9A	0,0	1,0	2,0	0,0	2,0
0·1 → 0·2	0D	0C	1D	8D	8C	9D	0,1	1,1	2,1		
0·2 → 0·3	3A	3B	2A	11A	11B	10A	0,2	1,2	2,2	0,2	2,2
0·3 → 0·4	3D	3C	2D	11D	11C	10D	6,3	1,3	2,3		
0·4 → 0·5	4A	4B	5A	12A	12B	13A	0,4	1,4	2,4	0,4	2,4
0·5 → 0·6	4D	4C	5D	12D	12C	13D	0,5	1,5	2,5		
0·6 → 0·7	7A	7B	6A	15A	15B	14A	0,6	1,6	2,6	0,6	2,6
0·7 → 0·8	7D	7C	6D	15D	15C	14D	0,7	1,7	2,7		

ETA / PHI

MCM NUMBER / CHANNEL

PHI +0·05 0·15 0·25

CPM LOGICAL ETA / PHI (0–3 / 0–15)

JEM LOGICAL ETA / PHI (0, 2, 4, 6 / 0, 2, 4, 6, 8, 10, 12, 14)

* NOTE THIS WOULD BE CORRECT IF THE JEM LVDS OUTPUT WERE SWITCHED TO THE CORRECT WAY ROUND — AS IT IS, THE PHI BITS ARE SWAPPED