ATLAS SCT – Operation of Barrel Modules:

Present and Future

The aims of this document are as follows:

1) To outline how modules have been operated to date in the system test, test beam and in institutes

2) As a discussion document, to help specify how modules may be operated in the final experiment

3) To identify areas in which further study is needed to ensure that the barrel module will perform adequately as part of the final system

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Distribution List

ATLAS SCT Steering Group

History of Changes

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0.1	08/11/01		First Draft
0.2	09/11/01		Additions from GFM
0.3	12/11/01		Minor editing
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0.6	07/12/01		Additions to section 2 (PWP) and section 3 (JGK)

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0 Introduction

1 Power up and Configuration

The power dissipated in the SCT front end electronics depends upon the settings of a number of DACs within the chips. The values of these DACs are undefined at power up. This forces us to consider together the issues of cooling, powering and configuring the modules.

1.1 The Present System

The scale of the systems of modules operated during system and beam tests thus far is smaller than the scale of the final SCT by two orders of magnitude. To date, liquid cooling has been used in lieu of the proposed evaporative system, making the cooling system more stable and easier to control. Under such circumstances the startup procedure is fairly straightforward: the procedure used in ATLAS is likely to be more complex.

In the present systems, the user must first start any external detector control system that may be in place[1], followed by the cooling system, then wait for the cooling system to stabilise. The cooling runs autonomously with the exception that, at the system test, systems are in place to detect and react to certain error conditions. Further details are given in section 5, “Interlocks and Detector Safety”.

From the DAQ console, the following sequence of actions is taken if the user calls the Startup procedure:

- Start the clock and configure the readout (VME) modules.
- If optical readout and control is in use, all necessary VcSELs are switched on.
- Low Voltage power is applied to each module in turn.
- Send Hard Reset to each module in turn.
- Send the configuration bitstream to each module in turn.
- Send global synchronous Soft Reset.

The ramping of the high voltage is left as a separate operation. It can therefore be initiated before or after the rest of the system has been configured at the discretion of the operator, but would normally be done now, after the modules have powered and configured.

The detector system is now configured and ready for use, although it is recommended to wait for the system to reach thermal equilibrium before making detailed analogue measurements. It may also be necessary to adjust the coolant temperature according to the specific investigation to be performed.

1.2 Current Issues

1.2.1 The “Warm Start” problem

1.2.1.1 SCTLV3 crash at CRATE power on

If SCTLV3 is cabled to a module when the VME crate is powered on, there is a high probability that the connected channel(s) will crash. Subsequent attempts to restart the affected channels are also more likely to fail if the modules are left connected, and during each attempted restart, the module will be subjected to a short pulse of magnitude up to 6 volts.

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[1] *An external DCS system is used at the system test, but not generally elsewhere.*

This is an accidental feature of the SCTLV3 design, and is under investigation by Jan Statsny. The problem will not be present in future designs. Meanwhile, the problem can be largely avoided by cycling the VME crate power only after the removal of all LV cables, and generally by leaving the VME crate power on as much as possible.

Note that this problem does not seem to occur at the barrel system test, only during bench tests. The reasons for this have yet to be understood.

1.2.1.2 SCTLV3 trips at MODULE power on

A module and support card present a dynamic load to SCTLV3, as opposed to a resistive one. During power up, instantaneous currents of up to 1.7A have been recorded on Vdd. Such transients can cause an overcurrent trip, in accordance with the LV3 specification.

These problems were investigated using a variety of barrel modules and an old support card fitted with 5V LVDS repeater chips. Trips could be avoided by setting the initial value of Vdd to be low, say 3.0V, waiting a short while, then raising Vdd to its nominal setting of 4.0V. With more recent support cards, fitted with 3.3V LVDS repeater chips, it is commonly found that ramping is not necessary as long as a valid clock signal is present. (If the clock signal is not present when a module with ABCD3TA chips is powered without ramping, SCTLV3 will trip every time – a useful diagnostic!)

A brief study of this problem was made at the system test using optical readout, during which similar transients were seen. This behaviour is correct according to the LV3 specification, and the workaround (ramping) is fairly simple. In light of this problem, and related issues outlined below, the specification of LV cards has now been revised such that the output voltages can be ramped up from zero volts.

1.2.2 The "Cold Start" problem

1.2.2.1 Testbeam

Problems were experienced when trying to operate certain modules at low temperatures during the testbeam held during August 2001. Some problems with LV trips occurred, generally specific to certain modules (0028 and 0018 on one LV3; K4_218): with the benefit of hindsight this would probably have been eliminated by ramping up Vdd in a few steps. In addition, some modules could not always be configured until they had been warmed. At this point they could be configured, and after subsequent cooling would continue to operate normally for several hours. It is not known if these problems were specific to irradiated modules, or in how many of the 9 modules they occurred.

For the October 2001 beamtest, Vdd was applied in two steps, 3.2V and 4.0V, practically eliminating problems of low voltage trips at startup. (There was a different problem most likely associated with an inadequate VME crate power supply, which is discussed below). No problems were observed with the cold configuration of modules. One possible reason for this difference is that the CLOAC module which generates the system clock had been replaced by a more recent one, which reduced the system clock jitter from perhaps 2nS to 1nS. Another possibility is that the problem was confined to some of the modules present in August which were not present in October (only the unirradiated modules 0029,0035 and 0036 were present in both beamtests; none of the five irradiated modules participated in both beamtests.)

This clock jitter observation would suggest that modules may have a different acceptance for the clock and command signals (amplitude, relative phase etc.) at low temperatures compared to that at room temperature. This may not be as much of an issue for the final experiment, with opto readout, as it is for the beam test, using electrical readout over long cables - but to the best of our knowledge, it is an area which has not been studied.

1.2.2.2 Irradiated modules B044 and B047

A second problem was noted in September during the post-anneal tests of irradiated modules B044 and B047. The modules, stored in a freezer at a temperature of -28^{O}C, could not be powered by SCTLV3. This is perhaps 20 ^{O}C lower than the operating temperature at the beam test. Switching to a bench supply the modules could be powered but the clock/2 signal was not observed until after a few tens of seconds, during which time the modules had warmed up by several degrees. At this point the modules could be transferred to SCTLV3, configured and operated normally.

It was later established that by using SCTLV3 to ramp up Vdd in small steps, it was in fact possible to warm these two modules from cold without tripping the supply. Once warmed by a few degrees, the full voltage could be applied and the modules functioned correctly.

Similar problems were again reported for modules B044 and B047 when operated in a freezer during their preparation for the October beamtest, but it is likely that the ramping procedure was not used. During the beamtest itself, using two-step ramping of Vdd (3.2V and 4.0V) at a higher temperature of around -10 ^{O}C, the modules could generally be powered without tripping.

1.2.2.3 Cold System Test

The first cold runs at the barrel system test, running 8 unirradiated modules at a temperature of -15C, took place during November 2001. A two step ramping procedure was used to apply Vdd, with the steps being set at 3.0V and 4.0V. One module gave rise to occasional LV trips, but this was equally true at room temperature, hence this minor difficulty is not a result of the reduction in the operating temperature. No problems were experienced with the cold configuration of these modules.

1.2.3 VME overload at HV switch on

During the beam test in October 2001, a strange problem was noted when using a particular 12 slot VME crate loaded with a total of six SCTLV3 cards, three SCTHV cards and one NI MXI-VME interface. Low voltage power could be provided without difficulty to all 12 SCT modules in the system, and each module could be configured. However, upon issue of the VME command to start the first high voltage channel, each and every LV channel would simultaneously trip off and the VME interface would crash. It was necessary to send the crate restart command to recover from this situation. The workaround was simple: if the high voltage was ramped whilst the low voltage was switched off, everything was fine.

The same problem was seen at the system test when using a VME crate rated to deliver 5A on the +/- 12V rails. Doubling the current capability of the power supply to 10A at +/- 12V, the problem went away.

It seems likely that a current surge is drawn from the +/- 12 volt rails each time a high voltage channel is started. When the low voltage channels are already switched on, these power rails are heavily loaded, and many VME crates are unable to cope with the increased demand. This highlights the provision of adequately powered VME crates as an on-going problem for small scale SCT test systems including the module Q/A facilities.

1.3 Considerations for the Final System

It is impossible to define a detailed startup procedure at the present time. One possible scenario for a single SCT barrel is given in the document ATL-IS-AP-0034, "Barrel Test Specification". The concepts behind this scenario are outlined below.

- The cooling is turned on to a number of cooling units[2]. (1)
- Low voltage power is applied to a number of modules serviced by each of those units. (8) The voltages may be ramped up from zero in small steps to avoid sudden changes in the heat load. Eventually the nominal value of Vdd is reached, but Vcc may be kept at the minimum value needed such that the modules can be configured.
- The DAQ issues the configuration bitstream to each of these modules. There may be a brief functional test of each module.
- If Vcc has been held at a minimal value for this group of modules, it is now ramped up slowly, allowing the cooling system to accommodate the changing heat load.

This procedure is then repeated until each cooling unit hosts a similar number of active modules, and then until every module of every cooling unit is powered and configured to its nominal operating conditions.

Some of the issues to be considered when defining a detailed startup procedure are highlighted in the following sections. (There may already be answers to some of these questions!)

1.3.1 Cooling/Mechanical

- What is the maximum instantaneous change in heat load that can be safely tolerated in each cooling unit?
- What time must be allowed for the system to stabilise after such a change?
- In what order should the modules be brought up to minimise mechanical deformations in the system?
- Is it safe to cool some loops and leave the others at ambient temperature before starting to power modules? (It might be necessary to have the adjacent cooling loops at an intermediate temperature.)

1.3.2 Chips and Modules

- What is the minimum value of Vcc needed such that a module may be configured? Does this vary as a function of irradiation?
- Are there any current spikes as the voltages are ramped up? (We know there are when using electrical readout, but the situation may be different with optical readout.)

1.3.3 DAQ/DCS

- Is startup under the control of DCS or DAQ?
  (This may be tied up with the transitions of the DAQ state machine, hence DAQ may have to be responsible for starting SCT.)
- Is the existing scheme for communication between DCS and DAQ adequate to meet our needs?

[2] *A single (barrel) cooling unit services 48 SCT modules.*

1.3.4 General

- How long does it take to power and configure the SCT detector?
  (Or: how long are we allowed to take to power and configure the SCT detector?)
- Has the startup scenario been adequately considered in the design of the interlock systems? Is it necessary to modify the interlock thresholds when starting the detector?

1.4 Suggestions for further study

Although most of the problems observed at startup have been related to current surges which exceed the trip level, and can be avoided by ramping, further studies in the following areas should be considered:

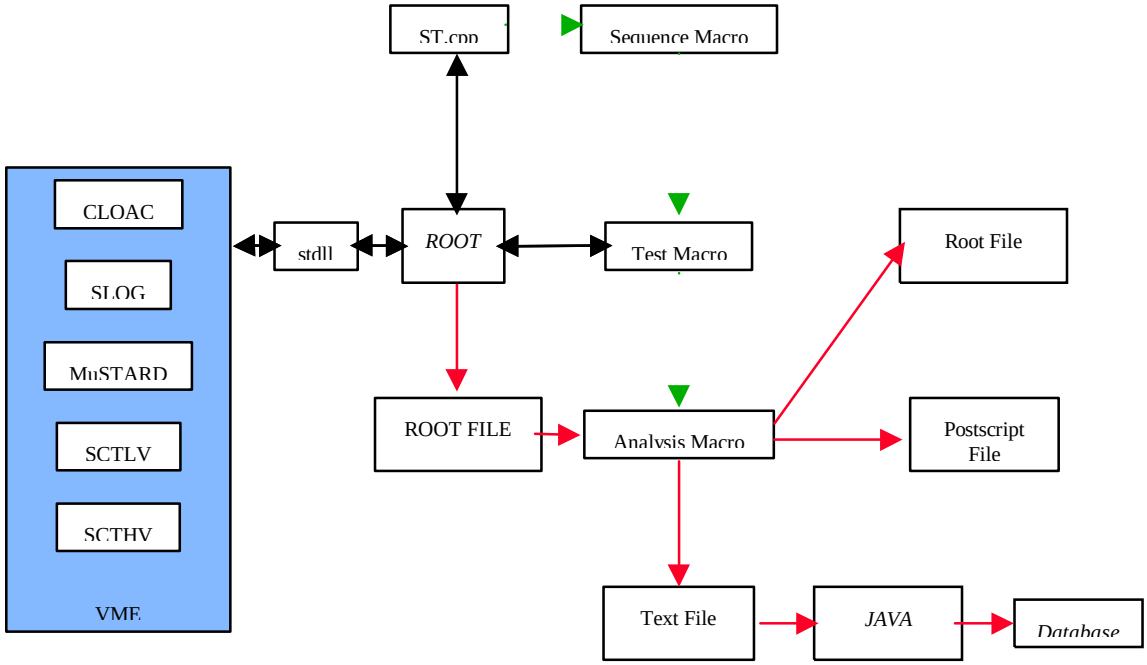
- Study of module Icc, Idd as f(temperature) (including startup spikes)
- Study of module clock/command phase margins as f(temperature)
- Study of module LVDS clock input margins (swing, offset) as f(temperature)

2 Characterisation and Debugging

2.1 The Present System

2.1.1 System Overview

One of the major objectives of the SCTDAQ software design was to provide sufficient flexibility to be able to devise and perform a new test without having to recompile large portions of the code. This has led to the architecture outlined below.



The following VME modules are used in the system:

- CLOAC - generates system wide clock and fast command signals
- SLOG - generates slow commands, including the configuration bitstream, and provides multiples copies of the clock and command signals
- MuSTARD - multichannel data receiver with histogramming capability
- SCTLV - low voltage power card
- SCTHV - high voltage power card
- OptIF - used in systems with optical readout to generate the biphase mark encoded clock and command streams and to convert the data returned by SCT modules from optical to electrical form

The basic routines that communicate with the hardware are implemented in the form of static libraries written in C. Higher level functions are implemented in a small number of C++ classes that are linked together with the static libraries, and some of the ROOT libraries, to form the dynamic link library stdll. This is the full extent of the compiled code: everything else runs through the CINT interpreter. The system is started by execution of the macro ST.cpp.

Many simple tests, such as a basic scan of any single parameter, can be defined and executed directly from the command prompt. More complex tests are implemented as discrete ROOT macros. In either case direct use is made of the functionality implemented within stdll and ST.cpp.

A test may first alter the setting of any number of variables affecting one or more modules within the system. Usually a number of scans are then defined and executed, taking the data needed to perform the test. A single scan algorithm is used for all scans, although different burst types and trigger types may be selected depending upon what the test seeks to accomplish. A brief description of the scan algorithm and some of the possible burst types is given below. At the end of each scan a ROOT file is generated containing the scan data for each module, records of error and event counters and some module configuration and DCS information.

Analysis of the data from each test is generally performed by a separate root macro whose outputs may include a postscript file, a root file and a text file. If the data is analysed on line, the macro may also update directly the configuration of the system of modules: for example, the contents of the trimdac registers of each chip may be updated following a study of the trimming.

2.1.2 The Scan Algorithm

The basic scan algorithm is outlined below:

```
Loop over (scan point){
     Set scanned variable
     If (cal pulse being sent){
           Loop over (cal line){
                 Set cal line
                 Send Configuration Sequence
                 Execute Trigger Burst of type selected by user or macro
     } else {
           Set cal line
           Send Configuration Sequence
           Execute Trigger Burst of type selected by user or macro
     }
     Present BURST histograms
}
Present SCAN histograms
```

The configuration sequence as used here includes the command to reprogram each register of every chip, with the exception of the TrimDAC commands which are sent only if the values need to be updated.

Trigger rates and the frequencies at which the Soft Reset and BC Reset commands are sent vary according to the type of Trigger Burst which has been selected and the settings of other system variables. A simplified description of a few common options is given in the following section.

2.1.3 Some types of Trigger Burst

2.1.3.1 TriggerBurst2

The basic (default) trigger burst is outlined below:

```
Send Soft Reset
While (nevents<target){
     Send configuration every x events   // default never
     Send soft reset every y events      // default every 1000 events
     Send BC reset every z events        // default never
     Send Trigger
     Wait until event has been decoded by MuSTARD
     If(errors){
           Read out event to host memory
           Parse event in software to identify causal stream
           BUT TAKE NO ACTION
     }
}
Copy MuSTARD histogram to host memory
```

In this mode of operation, we never study events recorded whilst the chips were being read out. This is about as far from ATLAS datataking as one can get, yet it remains the workhorse of gain and noise measurements in labs, at the system test and at the beam test.

2.1.3.2 DecodedBurst

In this mode of operation, each and every event is read out and processed in software, including histogramming. The algorithm is outlined below:

```
Send Soft Reset
While (nevents<target){
     Send configuration every x events   // default never
     Send soft reset every y events      // default every 1000 events
     Send BC reset every z events        // default never
     Send Trigger
     If(event in host memory){
           Decode event, identify errors and fill histograms
           If(event tree requested){
                 Fill the event tree
           }
     }
     Wait until event has been decoded by MuSTARD
     Read out event to host memory
}
Decode last event, identify errors and fill histograms
If(event tree requested){
     Fill the event tree
}
```

This burst type generates several histograms for each module in addition to the usual plots of occupancy against channel number. These include histograms of the occupancy per event for each side of a module and a plot showing the correlation in occupancy per event between the two sides. Optionally an event tree can be built and written to disk for offline analysis, such as the detailed study of common mode noise as outlined in section 3.1.1.1.

Once more, events are not recorded whilst the chips are being read out.

2.1.3.3 Vburst2

Vburst2, used during noise occupancy studies, is outlined below:

```
Send Soft Reset
While (nevents<target){
     Request burst of L1A triggers from CLOAC
     While (burst not complete){
           If (MuSTARD input FIFOs nearly full){
                 Suspend triggers until FIFOs are empty
           }
     Wait until FIFOs are empty
}
Copy MuSTARD histogram to host memory
```

CLOAC is set to issue a burst of L1A triggers at 100kHz frequency and to suspend the burst upon receipt of an external BUSY signal.

MuSTARD's registers are programmed such that BUSY is raised if, for any enabled stream:

- the input FIFO is almost full (less than 8k remaining)
- the number of triggers recorded exceeds the number of events received by more than 3

In this way we ensure that no data is lost due to buffer overflow at MuSTARD or in the ABCD readout buffer.

Data is acquired at a sustained trigger rate of 100kHz provided that the occupancy of **every** module in the system is lower than ~$2x10^{-2}$. At the nominal operating threshold of 1fC noise occupancy is 2-3 orders of magnitude lower than this, so ATLAS trigger rates are achieved.

This mode of running is used by the standard Noise Occupancy test, in use both in labs and at the system test. It is presently the only burst which has been written to provide protection against the possibility of overflow in the MuSTARD histogram memory, which occurs at 2^15. This is achieved by splitting large burst requests into several smaller ones, sampling the MuSTARD histogram at the end of each sub-burst. If the hit counter for a particular channel were to overflow at the end of burst (n), the normalised occupancy for that channel would be calculated as from the value of the hit counter (and the number of events recorded) at the end of burst (n-1).

2.1.4 Individual Tests

The following tests are examples of those which have been written to run within the exisiting system. Many of these tests are described in more detail in the document "Electrical Tests of SCT Hybrids and Modules". The list is not exhaustive, and must not be taken as a list of all the diagnostic tests which will be needed within the final SCT. Unless otherwise indicated, all tests make use of the basic scan algorithm and the default burst type, TriggerBurst2.

2.1.4.1 StreamDelay.cpp

This macro scans the relative phase of the data with respect to the system clock upon its arrival at MuSTARD. A known pattern is written to and read out from the modules. During the analysis phase the scan points which return good data are noted, and the phase is set to be at the centre of this region.

2.1.4.2 HardReset.cpp

This macro is used to ensure that each module responds correctly to the hard reset signal, that is, that the clock/2 signal is returned. No scanning is performed during this test, but an oscilloscope is required.

2.1.4.3 RedundancyTest.cpp

This macro is used to ensure that every chip on each module under test can be configured and read out using both the primary and redundant clock and command options. It is implemented as a scan of the variable "ST_SELECT".

2.1.4.4 FullBypassTest.cpp

This macro tests every option for the routing of data and the readout token between the chips of each module in the system. It is implemented as a scan of the variable "ST_TOKEN" which sets the modules to each of a number of predefined configurations, chosen to include every possibility.

2.1.4.5 PipelineTest.cpp

This macro identifies dead and / or stuck cells in the ABCD3T pipeline. A special trigger type is used which controls the number of BCOs between issue of a Soft Reset command and a L1A trigger. The test is implemented as a scan of this time interval.

2.1.4.6 StrobeDelay.cpp

This macro is used to adjust the setting of the strobe delay register. It is important to adjust this parameter each time a module is to be calibrated at a different temperature as the speed of the delay circuit varies as a function of temperature. The test first adjusts the threshold to a nominal 2fC level, then a scan is performed of the parameter "ST_DELAY" with a nominal 4fC charge injection.

2.1.4.7 ThreePointGain.cpp

This macro performs a series of three threshold scans for injected charges of nominal magnitude 1.5, 2.0 and 2.5fC. The gain, offset and noise are then calculated.

2.1.4.8 TrimRange.cpp

This macro studies the performance of the TrimDAC by performing a series of threshold scans with an injected charge of nominal magnitude 1.0fC for each of the four possible TrimRange settings. The TrimRange and TrimDAC settings are chosen to maximise the number of trimmable channels, and the modules are reconfigured to use these settings.

2.1.4.9 ResponseCurve.cpp

This macro performs a series of ten threshold scans for injected charges of nominal magnitude 0.50, 0.75, 1.00, 1.25, 1.50, 2.02, 3.00, 4.00, 6.00 and 8.00fC. The gain, offset and noise are then calculated.

2.1.4.10 NO.cpp

This macro measures the noise occupancy. In order to measure occupancy down to the level of 10^{-6}, up to 10^{6} events are recorded. At the other end of the scale, where occupancy approaches 1.0, only 2000 events are taken. Between these extremes the fractional occupancy of each channel is evaluated several times during each burst and the number of events recorded is varied such that, at each point of the scan, a minimum of 50 hits are seen in more than 50% of the active readout channels. The burst type "Vburst2" is used such that at low occupancies the trigger rate will be representative of that in ATLAS.

2.1.4.11 Timewalk.cpp

This macro studies the timewalk by means of a series of strobe delay scans for differing charges, each performed at a nominal threshold equivalent to 1.0fC.

2.2 Current Issues

None.

2.3 Considerations for the Final System

It is hoped that a system of similar flexibility can be devised using elements of the DAQ-1 system. A working document is under preparation.

2.4 Suggestions for Further Study

None at this time.

3 Datataking

3.1 The Present System

3.1.1 The System Test

The goal of the system test is to run a significant number of SCT modules in a physical configuration which is as close as possible to that planned for ATLAS, thereby testing the performance of the modules in such a system in comparison to their standalone performance. The basic operation of modules at the system test is largely as described in sections 1 and 2: modes of operation specific to the system test are outlined below.

3.1.1.1 Common Mode Noise

Every module in the system is set to a fixed threshold, usually 1.0fC, and DecodedBurst (see section 2.1.3.2) is used to issue a burst of L1A triggers. Each event is read out to host memory and decoded, the resulting hit pattern being stored in a ROOT tree. A large number of events are recorded, typically 10^6, to ensure sufficient statistics.

The ROOT trees are analysed offline to calculate a matrix of correlation between hits measured in different strips according to:

$$C_{ik} = (O_{ik} - O_iO_k)/\sqrt{(O_i-O_i^2)}\sqrt{(O_k-O_k^2)}$$

where C_{ik} is the matrix element representing strips i and k, O_i is the occupancy of trip i, and O_{ik} is the occupancy of a hypothetical AND of strips i and k.

The chip-by-chip summary of the correlation matrix, C', defined as the average over the diagonal of the respective chip-sub-matrix of the full matrix C_{ik}, is calculated for a chip-pair (m,n):

$$C'_{mn} = 1/N_{strips}*\Sigma_{i_m=k_n=1\ldots N_{strips}} C_{ik}$$

3.1.1.2 Long Term Stability

The long term stability of modules on the sector has been studied using two different methods:

Three-point gain measurement

This is the same measurement as described in section 2.1.4.7, but run repeatedly for several hours. Each measurement yields values for the gain and noise of each module: the variation in these parameters is studied as a function of time.

To date, the longest run has been of 8 hours duration.

Noise occupancy at a fixed threshold

The noise occupancy at 1fC threshold is studiesd using TriggerBurst2 (see section 2.1.3.1). Several short bursts are taken, each comprising 25000 triggers, and the resulting histograms are summed in software to provide statistics for typically 10^6 events. In this way the possibility of overflow of the MuSTARD histogram is avoided.

This procedure is repeated such that occupancy can be studied as a function of time. To date, the longest run has been of 30 hours duration.

3.1.1.3 Cold Running

In order to simulate the situation of running at low temperatures in ATLAS a *cryophasing* procedure has been established to safely cool down the whole sector to temperatures below zero, take data, and subsequently warm it up again. One important safety issue is the possibility that condensation may form on sensitive components on the sector (modules, opto-chips) so that during the whole cryophasing the dew-point is measured by the DCS system and used as a safety-limit (see section 5).

Cold operation is a prerequisite for the operation of irradiated modules on the sector due to the possibility of thermal runaway caused by the increased leakage currents drawn by irradiated detectors.

The cool down procedure is performed as follows:

- Put the sector into the freezer at room temperature and close and seal the cover.
- Flush sector and freezer with dry nitrogen to get down to low humidity.
- When a low humidity-plateau is reached start a slow cool-down.
- When the dew point is well below desired temperature turn on freezer and cool sector pipes to desired temperature.
- When desired temperatures are stable start measurements. Maintain ambient temperature via the freezer control.

The warm-up procedure follows these steps:

- Turn off freezer and stop chilling and start warm-up of pipe cooling liquid.
- When cooling pipes on sector reach room temperature start heating the freezer walls.
- When ambient temperature inside freezer is well above the dew point outside, the freezer cover can be opened.

This procedure has successfully been tested for ambient temperatures of -10^{o}C and pipe temperatures of -15^{o}C.

3.1.2 The Testbeam

3.1.2.1 Traditional Configuration (Analogue Telescope)

In the traditional beamtest, single-event readout is used, with a very large dead-time between events, due primarily to the time taken to read the Viking/VA2 chips of the analogue telescope. This is in the order of 10ms, depending on occupancy and noisy channels. Data-taking lasts the several seconds of the spill, 2.5 to 5.2s repeated every 15 to 17s depending on SPS conditions. The sequence is:

```
Start Run
Send Configuration Sequence
     Poll for Start of Spill
          Poll for Beam Trigger / Busy on
          Read one event from Mustards
          Read one event from IRAMs (telescope)
          Send Soft Reset
          Reset Busy
     Loop
Loop while (nevents<nevents_requested)
```

The software is organised in a very similar manner to SCTDAQ, and essentially executes as a macro from the ROOT interpreter, allowing, for example, fully automated threshold scans. All configuration and other module-related activities use standard SCTDAQ services.

3.1.2.2 High Rate Studies (Binary Telescope)

In the high-rate studies we aim to achieve more ATLAS-like readout conditions, eventually with dead-time-free operation. As initial steps in this direction, we have implemented in the October 2001 "LHC-like 25ns" beamtest a binary telescope using four SCT barrel modules in XY pairs. This permits tracking at a resolution adequate for most studies without the very long deadtime associated with Viking readout allowing a much higher readout rate. Although we still operated the system in single-event mode, we did explore instantaneous very high rate operation by implementing a multiple-trigger event. To do this, we defeated the limitations of CLOAC by using the register normally used for the calibration strobe pattern to send a sequence of 7 Level One Accepts (L1As), with an external delay unit used to delay the beam trigger to account for the pipeline length. This allowed, among other things, an attempt to measure the double-pulse resolution by looking for tracks in next-to-consecutive timebins in the same or neighbouring strips. Although not specifically aimed at studying the 'digital stability' at high, sustained trigger rates, it does exercise the output derandomising buffer.

Future beamtests are planned to explore more truly ATLAS-like data-taking conditions where triggers are allowed to propagate continuously unless throttle conditions are encountered, at high rates and for sustained periods, with Soft Resets and BC Resets at LHC rates. The essential difference from traditional operation, the dead-time-free nature of the dataflow, places great demands on the DAQ. Although the hardware, particularly MuSTARD, is quite capable of this kind of operation, the DAQ environment would need significant development and testing. In passing, one might mention that the very limited availability of modules severely limits this kind of development work.

3.2 Current Issues

Analysis of the recent beamtests is proceeding.

3.3 Considerations for the Final System

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3.4 Suggestions for Further Study

A number of SCT modules ought to be operated in ATLAS-like data-taking conditions, preferably with real beam, to allow an independent confirmation of the independence of efficiency on the various trigger and reset rates involved. This can be done using MuSTARD, preferably with optical readout (OptIF) to eliminate concerns of clock-command jitter on long cables. The TTC features implemented in CLOAC are probably sufficiently like those to be implemented in TIM that the full range of trigger and reset rates can be explored. However, in the near future we will have available final RODs and TIMs, with a significant DAQ development in the ATLAS DAQ-1 context. It would seem that a test of this nature would naturally and more productively be conducted as part of that effort. It would have a further benefit of providing a very direct focus for effort.

4 Error Recovery

4.1 The Present System

With the present system, the detector control and readout systems are largely integrated. Low voltage, high voltage, module clock/command and readout are all provided by VME modules interfaced to the same host computer. Under these circumstances recovery from certain error conditions, such as low voltage and high voltage trips, may be effected without involvement of an external DCS system.

4.1.1 LV Trip

At the start of each trigger burst, the DAQ detects any LV channels which may have tripped. Once the channels have been restarted, the full configuration sequence is sent to the modules to return them to operating conditions. Since this may increase the current drawn by the modules, and invoke further trips, LV trip recovery can become an iterative process.

Up to ten attempts are made to restart the tripped channels. Any channels which cannot be restarted, and which do trip again upon module reconfiguration, are simply switched off. The intention was to remove the modules associated with such "suspended" LV channels from the readout, but at the time of writing this functionality has not been implemented.

4.1.2 HV Trip

At the start of each trigger burst, the DAQ detects any HV channels which may have tripped. At the time of writing, the code to recover such channels has not been implemented.

4.1.3 Buffer Overflow

The chips are operated such that buffer overflow errors cannot occur, hence recovery is not necessary.

4.1.4 Synchronisation Errors

A mechanism has been coded to permit studies of synchronisation errors, but during most activites it is not used.

4.2 Current Issues

None.

4.3 Considerations for the Final System

4.3.1 LV Trip

Recovery from a low voltage trip may involve an interaction between the DCS and DAQ systems.

If the low voltage supply to a module fails, the ROD will detect that the module fails to respond to L1A triggers. Under such circumstances the error must be logged in the event header. Even if the DCS system is configured to recover LV trips automatically, we still have to reconfigure the module before it can be put back into the datastream. There will be restrictions as to which points in the run this may be done.

- Do we want DCS to attempt auto recovery of LV trips? Do we permit recovery during runs, or just between runs?
- How do we instruct DAQ to put a module back into the data stream? Are there restrictions upon when this can be done?
- Is the existing scheme for communication between DCS and DAQ adequate to meet our needs?
- What goes into the datastream if a module fails to respond?

4.3.2 HV Trip

Recovery from a high voltage trip may also involve an interaction between the DCS and DAQ systems.

If the high voltage supply to a module fails, the module will have increased occupancy. In the worst case, the ROD input pipeline may overflow. Under such circumstances the ROD will switch to "header only" mode for the affected streams, and data will be lost. In addition to this mechanism, we may wish to configure ROD to remove a module from the data stream if its mean occupancy exceeds a certain limit when averaged over a short period of time.

If the DCS system was configured to recover HV trips automatically, we may wish to send a message from DCS to DAQ to put the module back into the data stream. This is much simpler than the case of an LV trip, since we do not have to reconfigure the module.

- Do we want DCS to attempt auto recovery of HV trips?
- How long should DAQ wait before suppressing a noisy module?
- How do we instruct DAQ to put a module back into the data stream? Are there restrictions upon when this can be done?
- Is the existing scheme for communication between DCS and DAQ adequate to meet our needs?

4.3.3 Buffer Overflow

Buffer overflow errors will occur in ATLAS SCT. One recovery route will be by means of a soft reset synchronised to the ATLAS ECR signal, which will occur no less often than once every 160 seconds. (ECR rates of up to 1 per second have been discussed in the past.)

This condition will also be detected by ROD: it may be possible to issue an explicit soft reset to a module to recover from this error.

4.3.4 Synchronisation Errors

Synchronisation errors will occur in ATLAS SCT. One recovery route will be by means of a soft reset synchronised to the ATLAS ECR signal, which will occur no less often than once every 160 seconds. (ECR rates of up to 1 per second have been discussed in the past.)

This condition will also be detected by ROD: it may be possible to issue an explicit soft reset to a module to recover from this error.

4.4 Suggestions for Further Study

None at this time.

5 Interlocks and Detector Safety

5.1 The Present System

The following safety system has been implemented at the system test, but is not generally used elsewhere.

A detector control system (DCS) has been implemented using LabVIEW. Its direct inputs include a number of ambient temperature sensors, temperature sensors connected to the module cooling pipes, humidity sensors within the thermal enclosure and a nitrogen flow sensor at the gas input to the enclosed volume. The system is also connected to the chiller such that the set point can be controlled and the temperature of the cooling liquid can be monitored.

A second LabVIEW application runs on the DAQ computer, and is able to read directly the module temperatures measured by the low voltage cards. A TCP/IP link is used to pass this information back to the DCS system. Using a second TCP/IP connection, the DAQ system is able to query the status of certain DCS parameters. This latter mechanism is periodically used by the DAQ to check the status reported by the DCS system: if an alarm condition has been noted, a controlled shutdown is initiated.

The DCS system has three alert levels:

- "Warning" - parameters have exceeded the lowest warning level. No action is taken.
- "Alarm" – parameters have exceeded the second warning level. A controlled shutdown is initiated.
- "Fatal" – parameters have exceeded the highest warning level. The interlock is invoked.

At the time of writing, both the controlled shutdown and the interlock operate only upon the low voltage supplies. Should a fatal warning remain unacknowledged for some time, email and SMS messages are sent to the person on shift duty. A summary of error conditions is given below.

Note that this implementation is somewhat different from that in the final experiment, where it should be possible to execute a controlled shutdown (but not startup) without involvement of the DAQ system.

5.1.1 Over Temperature

This alarm is set if any module or pipe sensors exceed a specified limit. A three-minute period is allowed during which the DAQ system may query the DCS system, discover the alarm condition and begin a controlled shutdown.

If the DAQ does not begin a controlled shutdown within this three-minute period, or if the alarm escalates to "fatal" status, the hardware interlock is invoked, immediately shutting down the low voltage supplies. The interlock condition is maintained until it has been cleared by the operator at the DCS console.

5.1.2 Chiller Failure

If the DCS system loses contact with the chiller system, the interlock is invoked such that all low voltage power is cut immediately. The interlock condition is maintained until it has been acknowleged by the operator at the DCS console.

5.1.3 Dew Alarm

This alarm is invoked if any of the following conditions apply:

- the pipe or module temperatures approach the dewpoint as calculated from the known humidity within the thermal enclosure
- the humidity exceeds a specified limit
- the nitrogen gas flow falls below a minimum value.

Upon such an alarm, the chiller set point is raised to 20^{o}C and manual intervention at the chiller control panel is disabled. A three-minute period is allowed during which the DAQ system may query the DCS system, discover the alarm condition and begin a controlled shutdown.

If the DAQ does not begin a controlled shutdown within this three-minute period, of if the alarm escalates to "fatal" status, the hardware interlock is invoked, immediately shutting down the low voltage supplies. The interlock condition is maintained until it has been cleared by the operator at the DCS console.

5.1.4 DCS crash

If DAQ finds that the DCS system no longer responds to its requests, a controlled shutdown is initiated.

5.2 Current Issues

5.2.1 Controlled Shutdown

The controlled shutdown taken in response to a DCS alarm should be expanded to include a shutdown of the high voltage supplies in addition to the low voltage supplies.

5.3 Considerations for the Final System

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5.4 Suggestions for Further Study

None at this time.

6 System Shutdown

6.1 The Present System

From the DAQ console, the following sequence of actions is taken if the user calls the Shutdown procedure:

- The Low Voltage is switched off, each module in turn.
- The High Voltage channels are ramped down in parallel, and then switched off.
- If optical readout and control is in use, all VcSELs are switched off.

It is left to the user to switch off the cooling system, if necessary.

6.2 Current Issues

None.

6.3 Considerations for the Final System

A shutdown procedure cannot be stated until a detailed startup procedure has been defined.

Naievely, one might expect a controlled shutdown procedure to be pretty much the reverse of the startup procedure.

6.4 Suggestions for Further Study

None at this time.